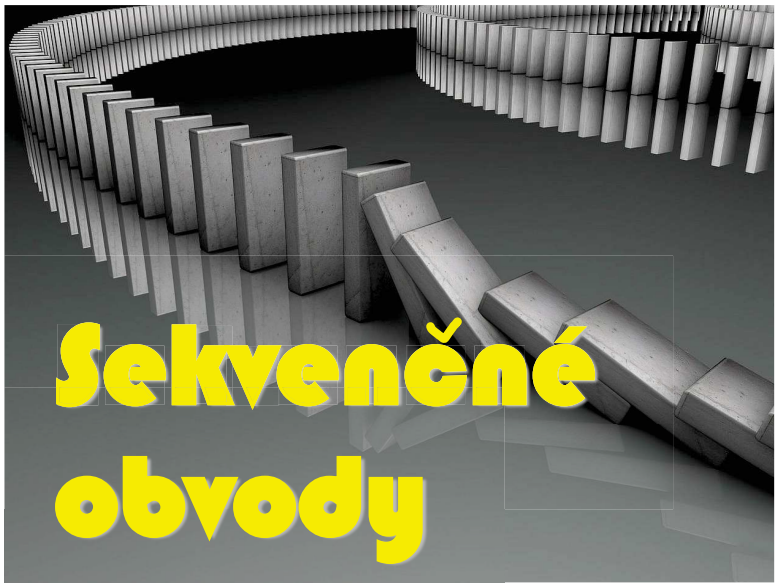
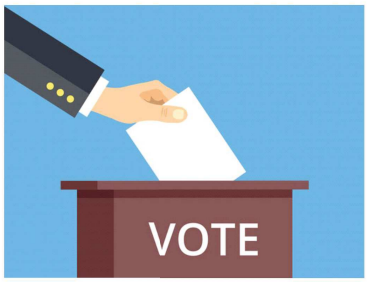
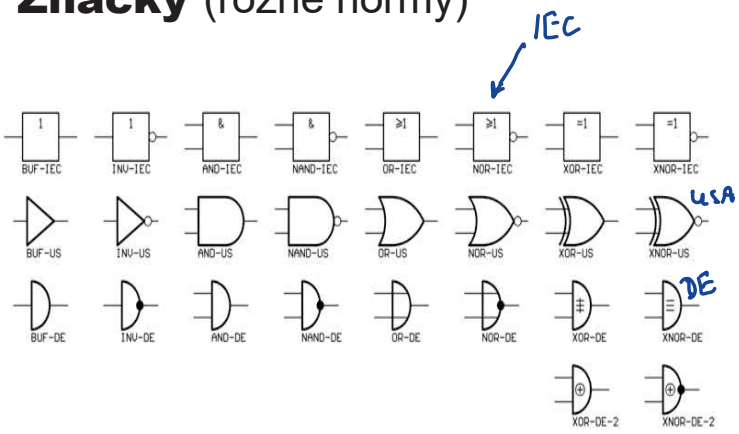


sli.do #ZPOC



Info: v týždni 28.10 – 1. 11. 2019 **nebudú** cvičenia ani prednáška!

Značky (rôzne normy)



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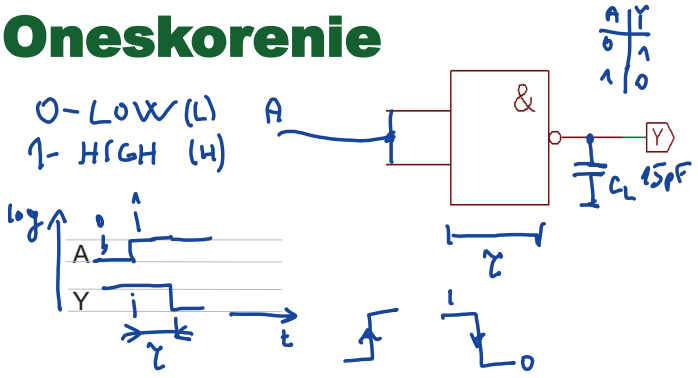
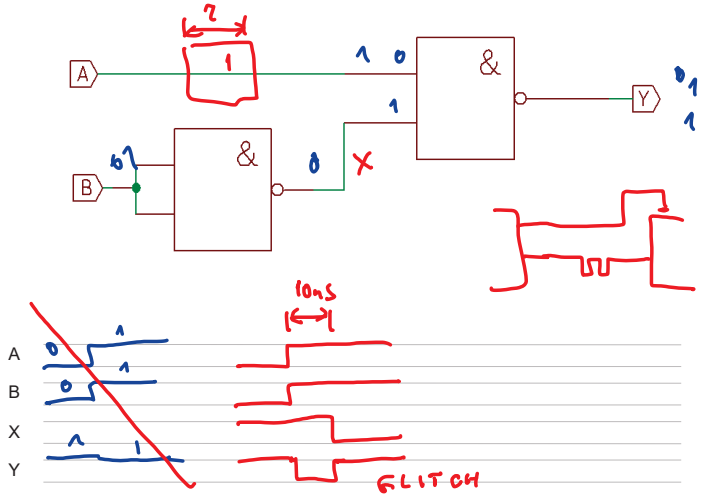


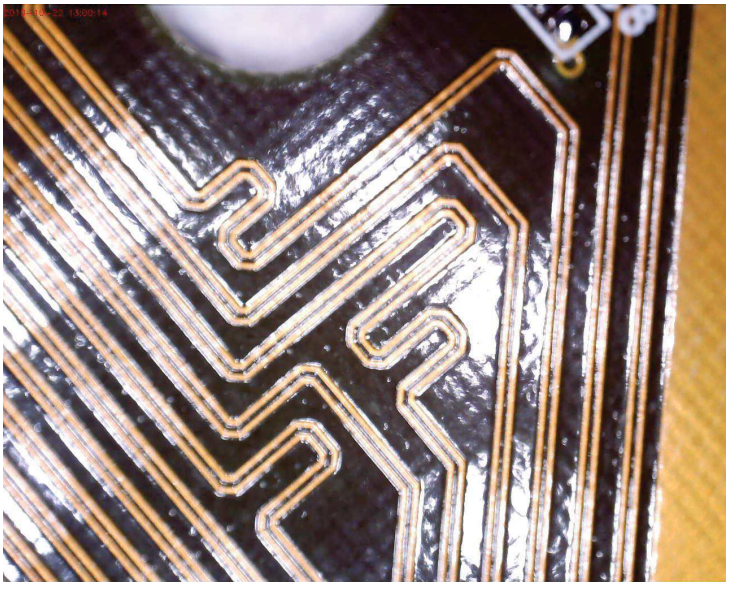
Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	15	ns

Oneskorenie





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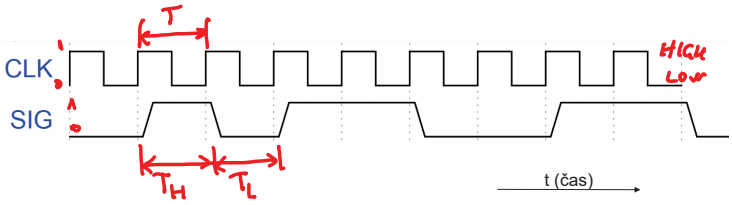
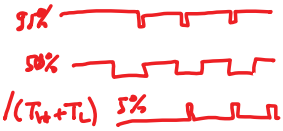
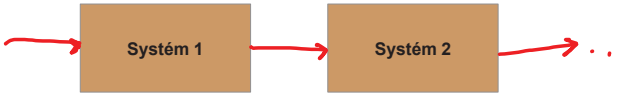


perióda (period) $T = T_H + T_L$
frekvencia (frequency) $f = 1/T$
plnenie (duty cycle) $DC = T_H/T = T_H/(T_H+T_L)$

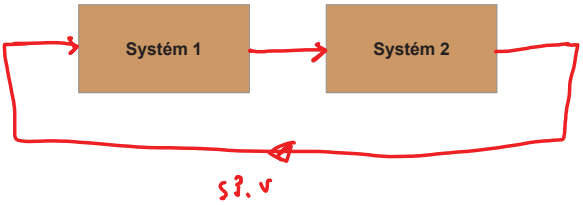


Spätná väzba feedback

Otvorená slučka



Uzavretá slučka

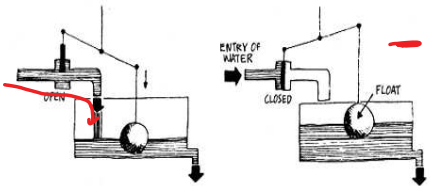


Spätná väzba feedback

Kladná (pozitívna) spätná väzba

+

Záporná (negatívna) spätná väzba



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Spätná väzba feedback

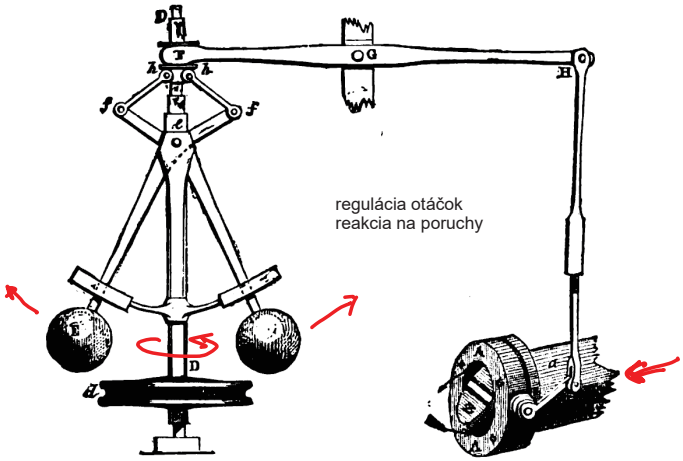
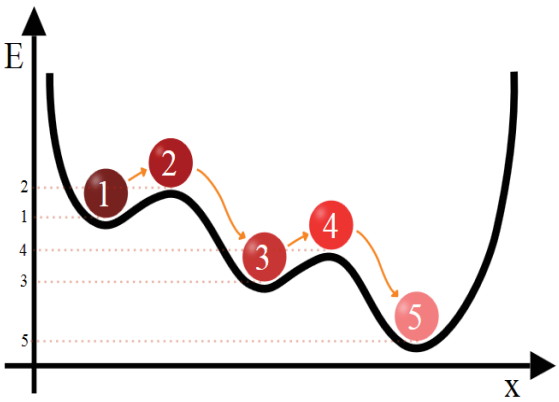


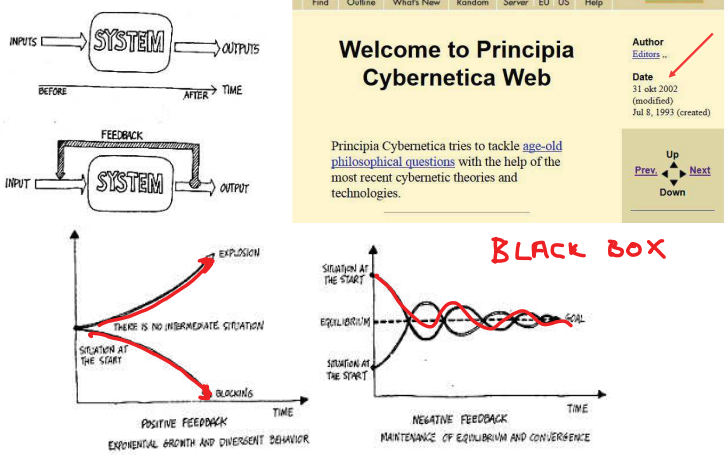
FIG. 4.—*Governor and Throttle-Valve.*

Stabilita



Kybernetika

http://pespmc1.vub.ac.be/



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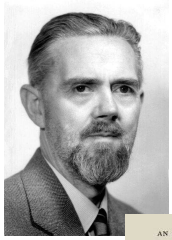
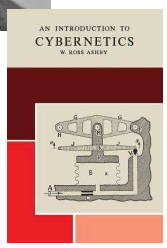
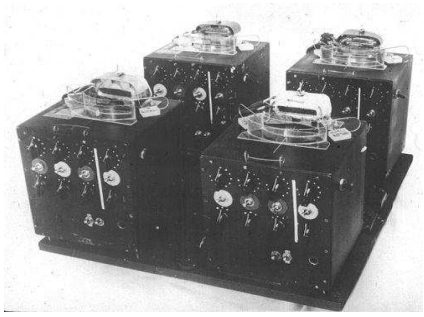
W. Ross Ashby (6. 9. 1903 – 15. 11. 1972)





Anglický psychiater a pionier kybernetiky

Kybernetické systémy živé aj neživé



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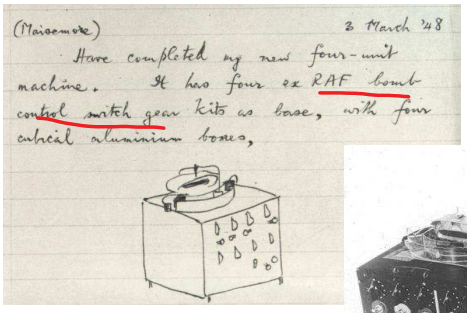
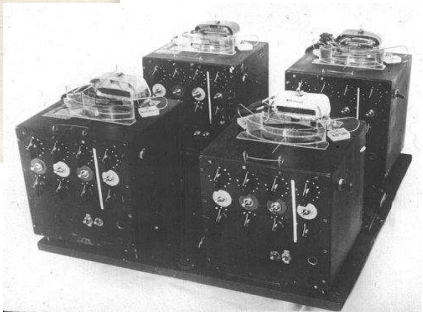
W. Ross Ashby (6. 9. 1903 – 15. 11. 1972)





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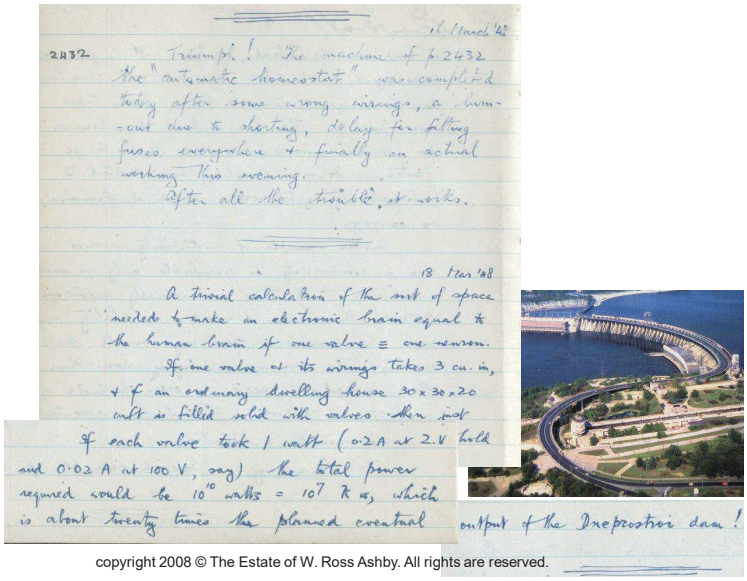

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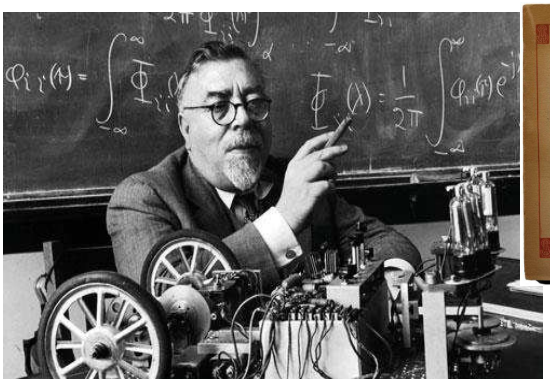
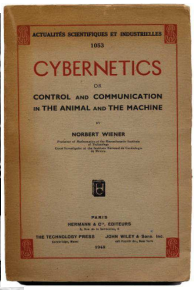
Norbert Wiener (26.11.1894 – 18. 3. 1964)





Americký matematik a filozof.
Stochastické procesy, šumy, komunikačné systémy, riadiace systémy a kybernetika

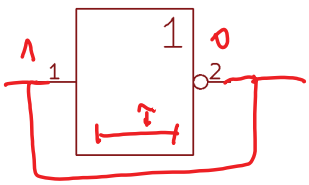
Kybernetika

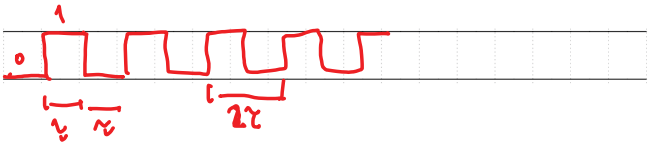
M. Rozental, P. Judin: Stručný filozofický sloník, SNPL, 1955

Kybernetika (ze starořeckého slova s významem řídící) - reakční pavěda, která vznikla v USA po druhé světové válce a značně se rozšířila i v jiných kapitalistických zemích; forma soudobého mechanicismu. Stoupenci kybernetiky ji definují jako universální vědu o spojích a komunikacích v technice, o živých organismech a o společenském životě, o "všeobecné organisaci" a řízení všech procesů v přírodě a ve společnosti. Kybernetika tak ztotožňuje mechanické, biologické a sociální vzájemné souvislosti a zákonitosti. Kybernetika jako každá mechanistická theorie popírá kvalitativní specifičnost zákonitostí různých forem existence a vývoje hmoty a redukuje je na mechanické zákonitosti. Kybernetika vznikla na základě moderního rozvoje elektroniky, zejména nejnovějších mechanisovaných počítacích strojů, automatiky a telemechaniky. Na rozdíl od starého mechanicismu 17.-18. století nezkoumá kybernetika psychofysiologické a sociální jevy analogicky s nejjednoduššími mechanismy, ale s elektronovými stroji a přístroji; ztotožňuje práci mozku s prací počítacího stroje a společenský život se systémem elektrod a radiokomunikací. Svou podstatou směřuje kybernetika proti materialistické dialektice, proti moderní vědecké fysiologii, kterou založil I. P. Pavlov (viz), a proti marxistickému, vědeckému pojetí zákonů společenského života. Tato mechanistická metafysická pavěda se výtečně snáší s idelalismem ve filosofii, psychologii a sociologii.

Kybernetika jasně vyjadřuje jeden z hlavních rysů buržoasního světového názoru, jeho nelidskost a snahu přeměnit pracující v součástku stroje, ve výrobní nástroj a nástroj války. Zároveň je pro kybernetiku charakteristická imperialistická utopie, podle níž má být živý, myslící člověk, jenž bojuje za své zájmy, nahrazen ve výrobě i ve válce strojem. **Podněcovatelé nové světové války využívají kybernetiky pro své špinavé praktické zájmy.** Pod rouškou propagandy kybernetiky jsou v imperialistických zemích badatelé z nejrůznějších oborů zatahováni do přípravy nových prostředků masového vyhlazování lidí - elektronové, telemechanické a automatické zbraně, jejíž konstrukce a výroba se rozrostly na obrovské odvětví válečného průmyslu kapitalistických zemí. Kybernetika je tedy nejen ideologickou zbraní imperialistické reakce, ale i prostředkem k uskutečňování jejích agresivních válečných plánů.

Spätná väzba
v logických obvodoch





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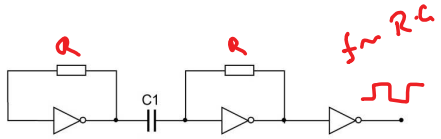

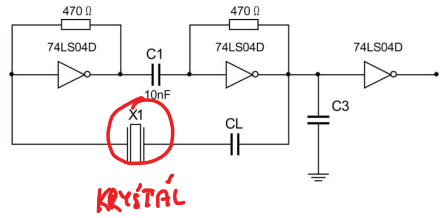

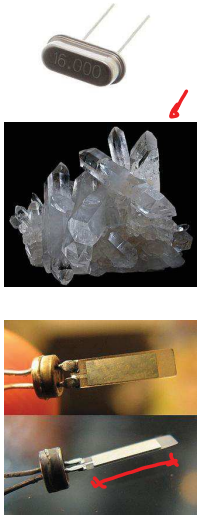

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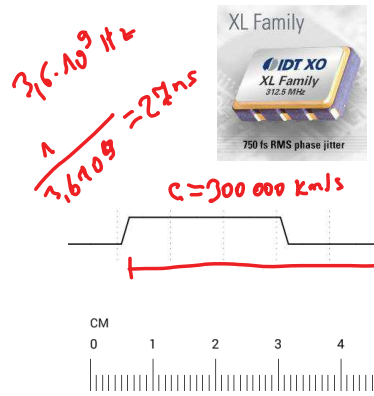
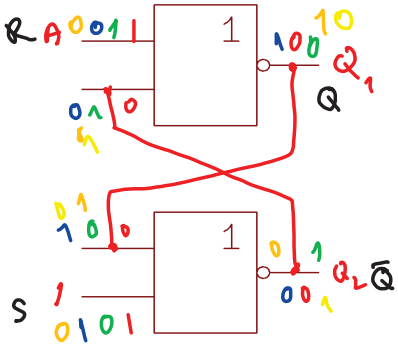
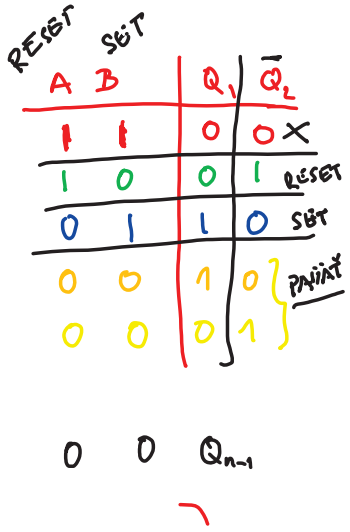


RS
preklápací obvod

flip flop





RS
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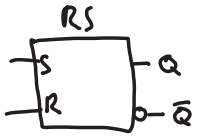
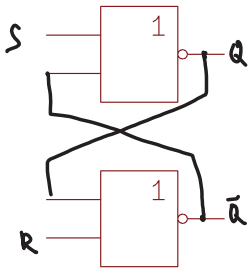


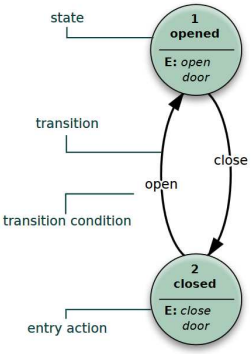
Q_n	S	R	Q_{n+1}	Pozn.
0	0	0	0	Pamätá si
1	0	0	1	Pamätá si
0	0	1	0	Reset
1	0	1	0	Reset
0	1	0	1	Set
1	1	0	1	Set
0	1	1	X	Undefined
1	1	1	X	Undefined

RS NOR
preklápací obvod

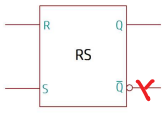


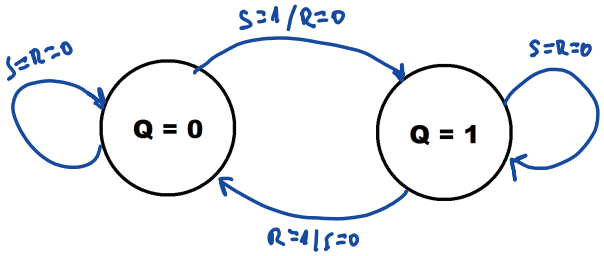
R-S preklápací obvod

Stavový diagram

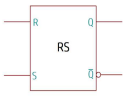


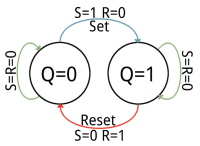
RS NOR
stavový diagram



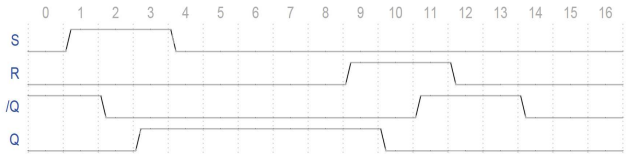


RS NOR
rozličné formy zápisu



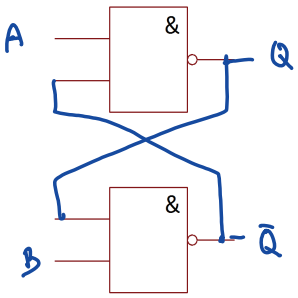


Q_n	S	R	Q_{n+1}	Pozn.
0	0	0	0	Pamätá si
1	0	0	1	Pamätá si
0	0	1	0	Reset
1	0	1	0	Reset
0	1	0	1	Set
1	1	0	1	Set
0	1	1	X	Undefined
1	1	1	X	Undefined



R-S preklápací obvod

RS NAND
preklápací obvod



Synchrónny RS
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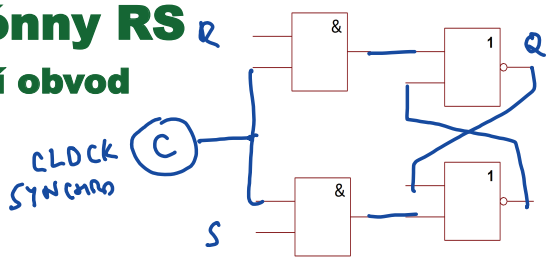

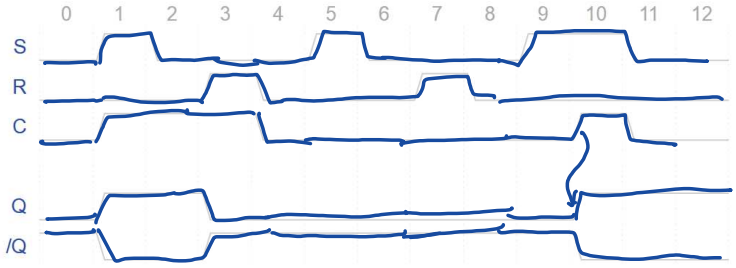

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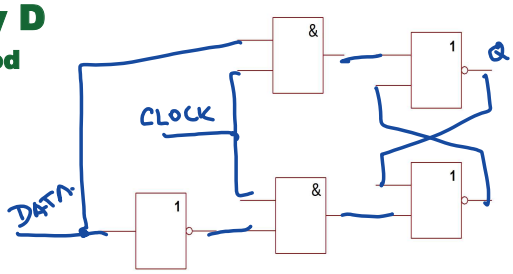
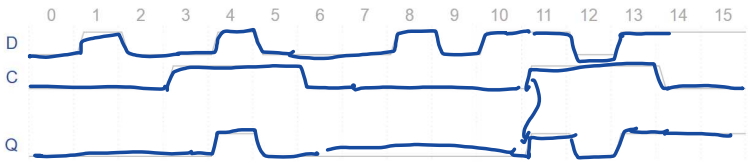
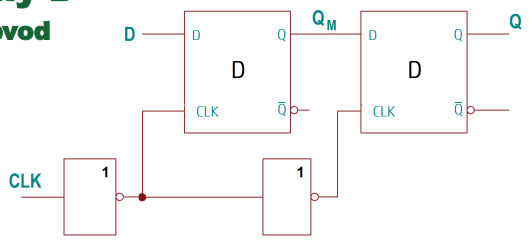
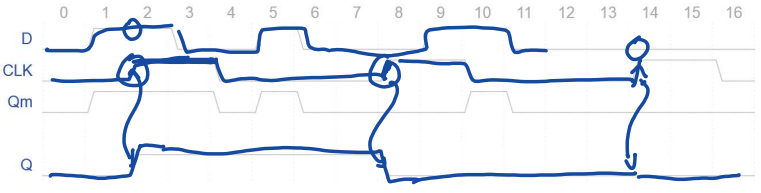


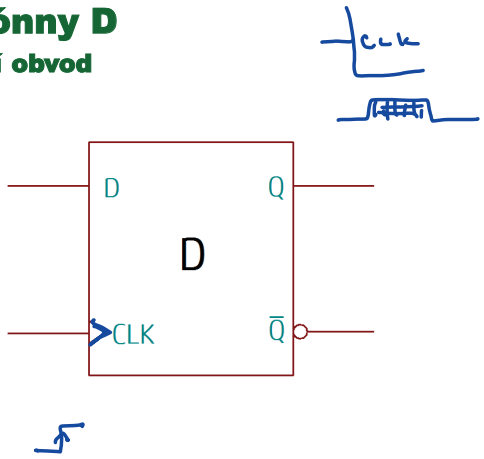


Synchrónny D
preklápací obvod





Synchrónny D
preklápací obvod



SN5474, SN54LS74A, SN54S74
SN7474, SN74LS74A, SN74S74
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR
SDLS119 – DECEMBER 1983 – REVISED MARCH 1988

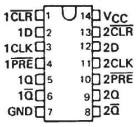
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

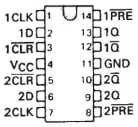
These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

SN5474 . . . J PACKAGE
SN54LS74A, SN54S74 . . . J OR W PACKAGE
SN7474 . . . N PACKAGE
SN74LS74A, SN74S74 . . . D OR N PACKAGE
(TOP VIEW)



SN5474 . . . W PACKAGE
(TOP VIEW)



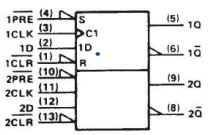
SN54LS74A, SN54S74 . . . FK PACKAGE

FUNCTION TABLE

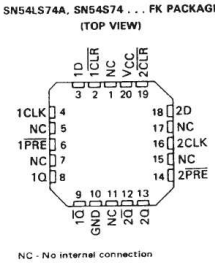
INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

† The output levels in this configuration are not guaranteed to meet the minimum levels in V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

logic symbol‡

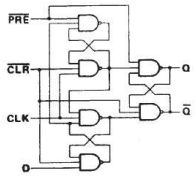


‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.



NC - No internal connection

logic diagram (positive logic)



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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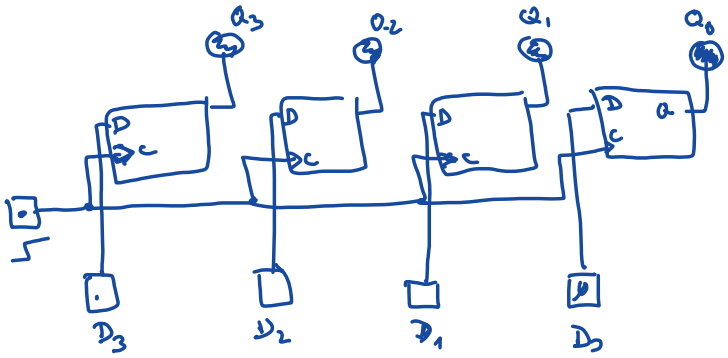
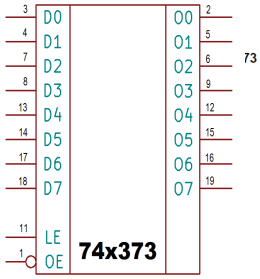
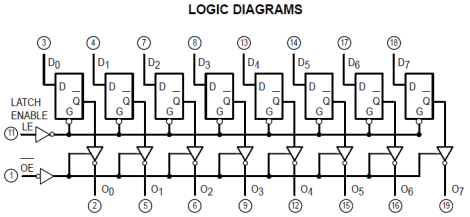
Pamäťový register



Pamäťový register 74x373



LOGIC DIAGRAMS



LS373

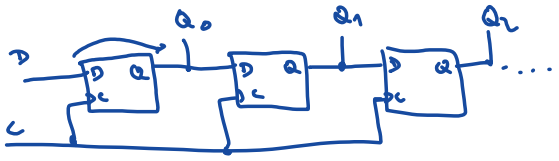
D_n	LE	OE	O_n
H	H	L	H
L	H	L	L
X	L	L	Q_0
X	X	H	Z*

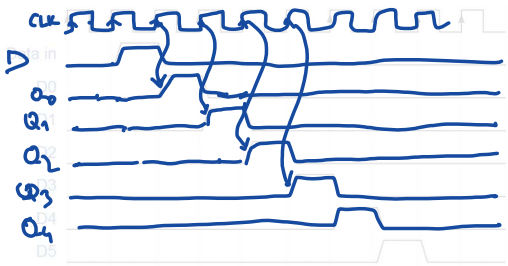
D0 – D7 Data Inputs

LE Latch Enable (Active HIGH)
CP Clock (Active HIGH going edge)
OE Output Enable (Active LOW)

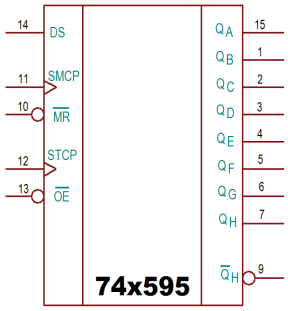
O0 – O7 Outputs

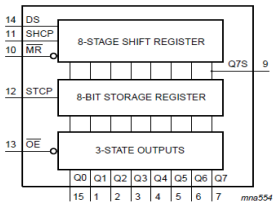
Posuvný register





74HC595





DS – serial data input

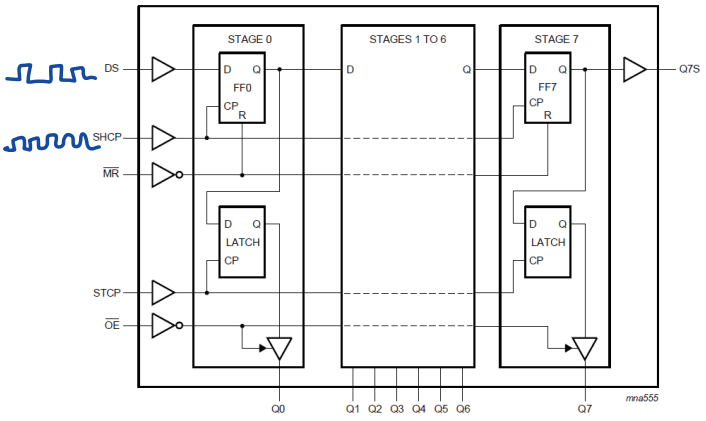
QA – QH – parallell data output

/QH – serial data output

/OE – output enable
/MR – master reset

SMCP – shift register clock input
STCP – storage register clock input

74HC595



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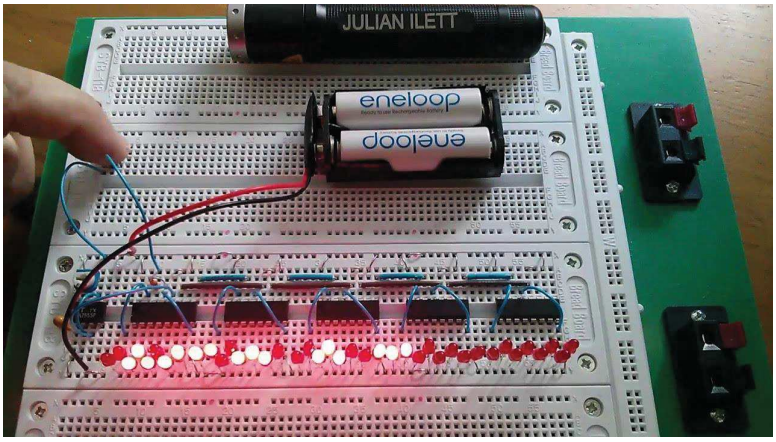
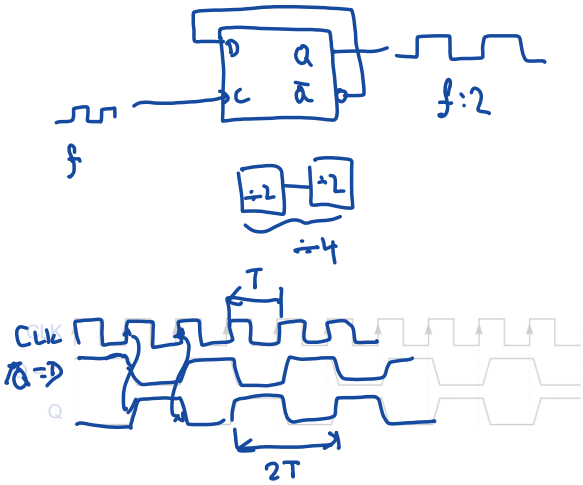
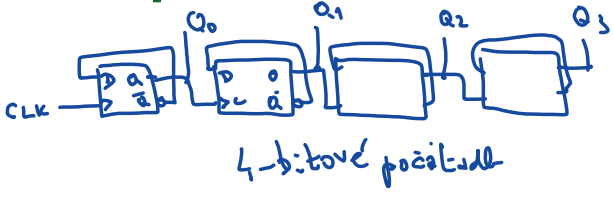
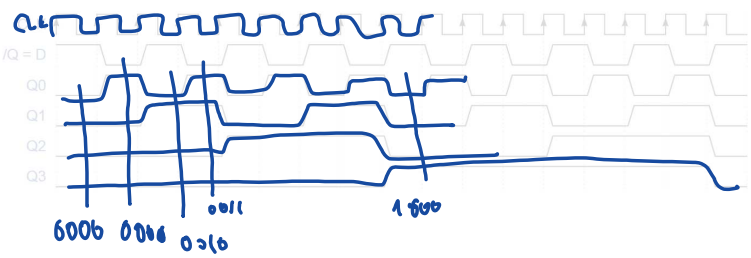


Delička frekvencie

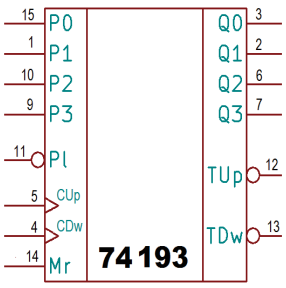


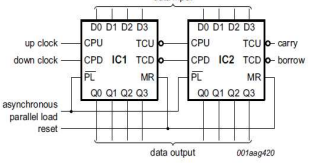
Binárne počítadlo

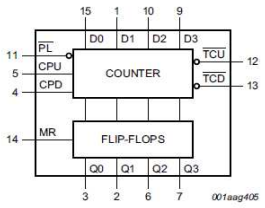




74LS193







P0 – P3 data input
Q0 – Q3 data output

/PL – async. Parallell Load
MR – async. Master Reset

Cup – count UP
Cdw – count DOWN

Tup – Terminal (carry) UP
Tdw – Terminal (carry) DOWN

74LS193

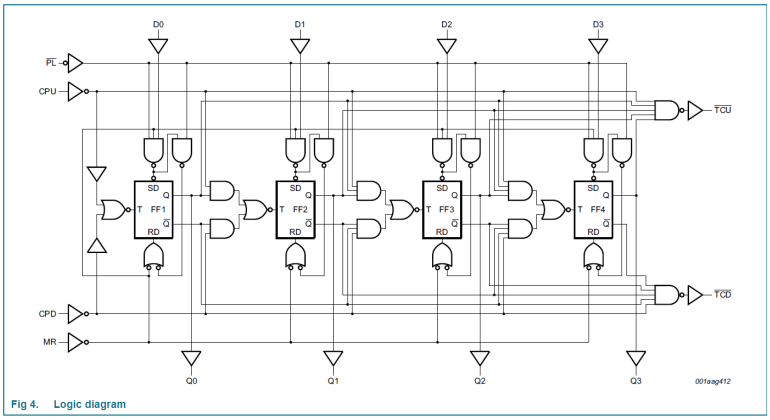


Fig 4. Logic diagram

Domáca úloha

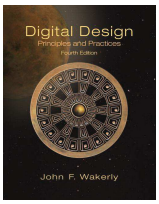
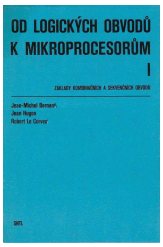
Zoberte ľubovoľné 4-ciferné binárne číslo a vydeľte ho 2, potom 4 a napokon 8.

Čo dostanete?

Vedeli by ste navrhnúť HW deličku 2^n ?

Chcem vedieť viac...

John F. WAKERLY:
Digital design.
Stanford University : Prentice Hall, 2006.



Jean-Michel BERNARD, Jean HUGON
a Robert Le Corvec:
Od logických obvodů k mikroprocesorům.
SNTL : Praha, 1982