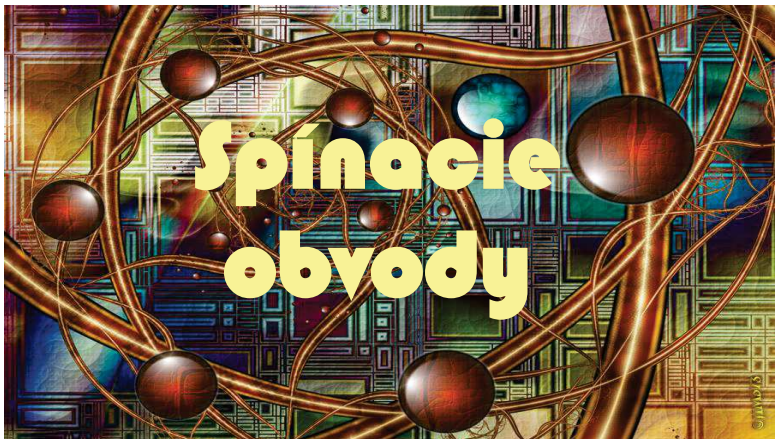
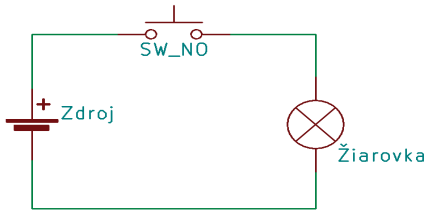


Spínač

Source: Wikipedia

Spínač

Spínač



Tabuľka

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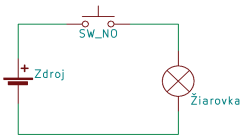
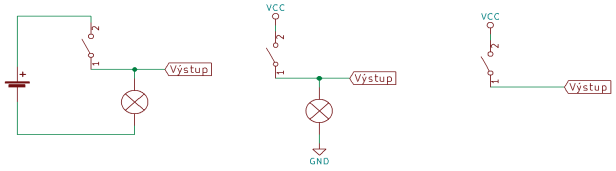
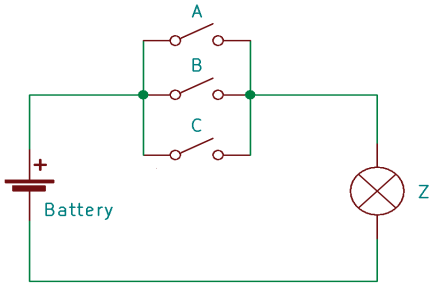
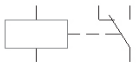


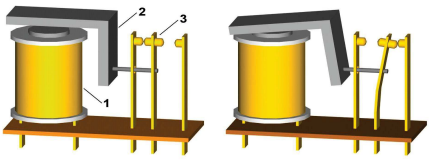


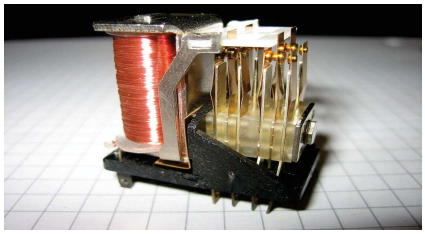
Logický súčet viac premenných OR



Relé







1. Cievka (coil)
2. Kotva (armature)
3. Kontakt (contact)

Source: Wikipedia

sli.do #ZPOC

Koľkokrát môže relé zopnúť kým sa pokazí?

Panasonic
ideas for life

MINI-ISO AUTOMOTIVE RELAY | **CB RELAYS**

FEATURES

• This relay has an Mini-ISO (International Organization for Standardization) terminal arrangement.
• Relay is compact and high capacity (40 A).
Compact form factor realized with space saving 22 × 26 mm .866 × 1.024 inch small base area thanks to integrated bobbin and base construction. Features high switching capacity of 40 A

TYPICAL APPLICATIONS

• Automobiles
Headlights, Cell motors, Air conditioners, ABS, EPS, etc.
• Construction equipment
• Agricultural equipment, Conveyor, etc.

characteristics	Vibration resistance	Functional	10 Hz to 500 Hz, Min. 44.1m/s² {4.5G}
		Destructive	10 Hz to 2,000 Hz, Min. 44.1m/s² {4.5G} Time of vibration for each direction; X, Y, Z direction: 4 hours
Expected life	Electrical (at nominal switching capacity)		Flux-resistant type: Min. 10^5, Sealed type: Min. 5×10^4 (Operating frequency: 2s ON, 2s OFF)
	Mechanical		Min. 10^6 (at 120 cpm)
	Conditions for operation, transport and storage*2		Standard type; Ambient temperature: -40 to +85°C -40 to +185°F, Humidity: 5 to 85% R.H. (Not freezing and condensing at low temperature)

Claude Elwood Shannon

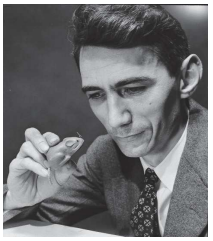
* 30. apríla 1916, Michigan
† 24. február 2001, Massachusetts

– profesor na MIT

Kybernetika, Teória informácie, Entropia

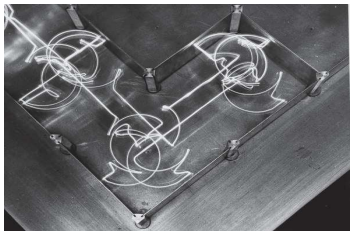
Symbolická analýza zmeny a spínacie obvody

Bell Labs Inc. - reléová logika



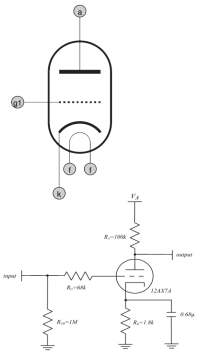
Source: Wikipedia, http://cyberneticzoo.com

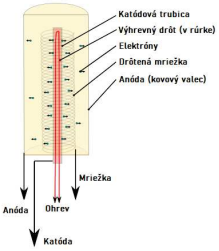
Theseus:
Maze-Solving Mouse (1952)



Source: http://cyberneticzoo.com

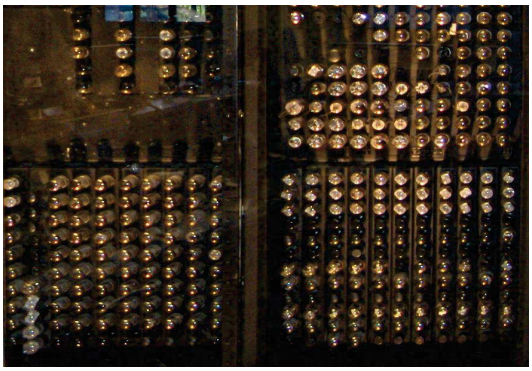
Elektrónka





Source: Wikipedia

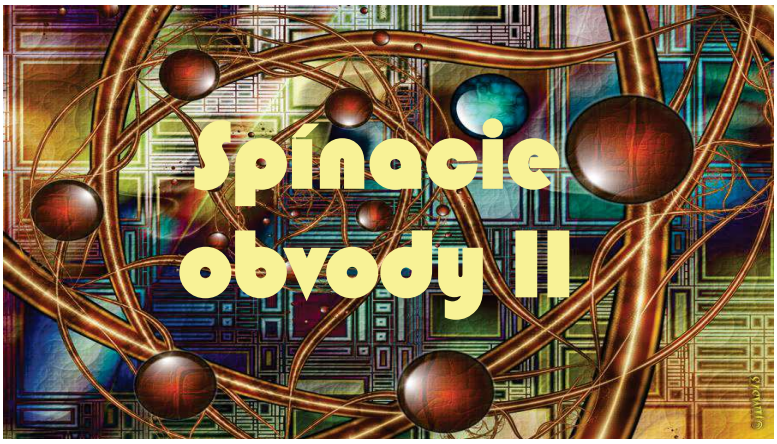
Elektrónka



ENIAC

- r. 1946
- 17,468 elektróniek
- P =150 kW
- m = 27 000 kg
- 2,4 × 0,9 × 30 m
- $487,000
  (ekv. 2016: $6,740,000)

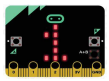
Source: Wikipedia



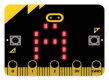
micro:bit 2

Úlohy na cvičenie:

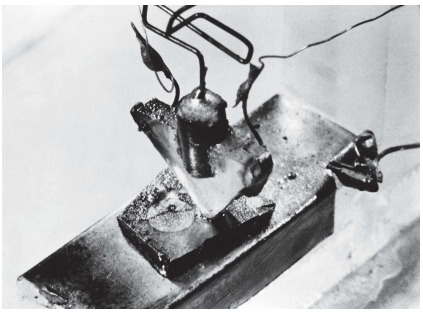
* **Naprogramujte hru kameň, papier, nožnice**
* **Naprogramujte aspoň dve rozličné logické funkcie premenných A a B**



* **Naprogramujte tester reakčnej doby**



Tranzistor



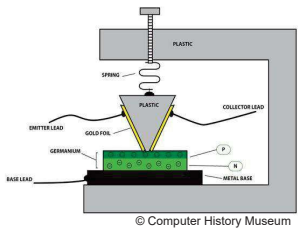
Bell Labs

John Bardeen, Walter Brattain, a William Shockley

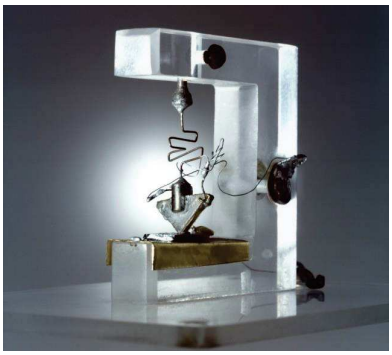
Nobelova cena 1956

Source: Wikipedia

Tranzistor



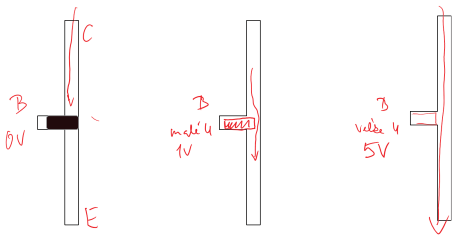
© Computer History Museum



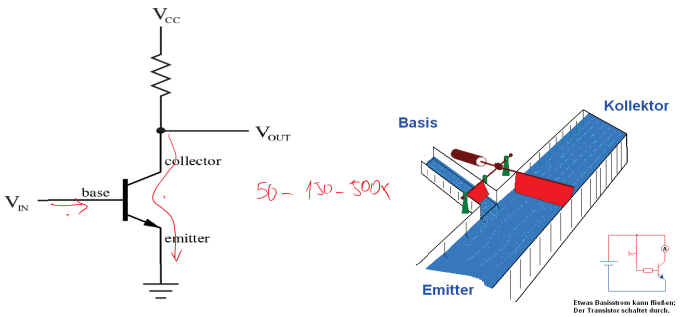
Source: Wikipedia

1939: William Shockley (AT&T's Bell Labs) myšlienka náhrady elektróniek
1947: Shockley -> John Bardeen and Walter Brattain prvý reálny tranzistorový zosilňovač
1956: Nobelova cena pre všetkých troch

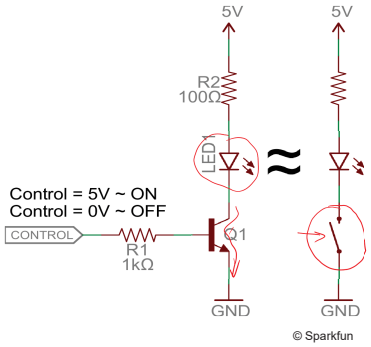
Tranzistor



Tranzistor bipolárny



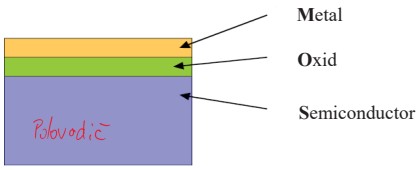
Tranzistor



Tranzistor unipolárny

Súčasné počítače využívajú unipolárne tranzistory

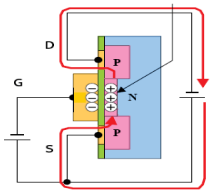
FET – Field Effect Transistor

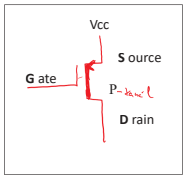


Metal **O**xid **S**emiconductor (MOS)

PMOS (MOS tranzistor s kanálom P)

- historicky najstaršia technológia:
- nevýhody: nízka rýchlosť a zlá zlučiteľnosť s TTL obvodmi

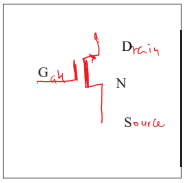


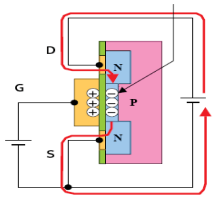


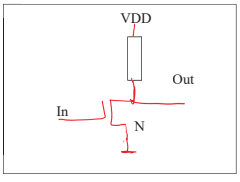
Náhrada: NMOS (MOS tranzistor s kanálom N).

Technológia NMOS

+ rýchlejšie,
+ zlučiteľné s TTL
- Nevýhody: „straty“



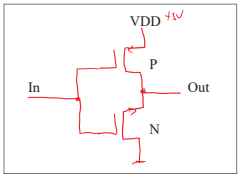




Náhrada: CMOS

Technológie CMOS (Complentary MOS)

Výhody:
minimalizované straty
zlučiteľné s TTL

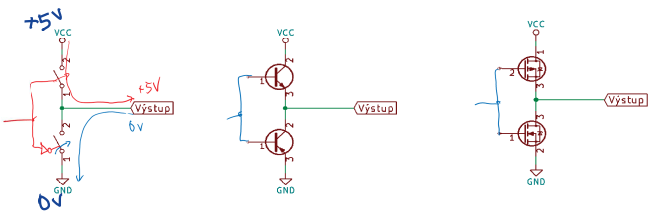


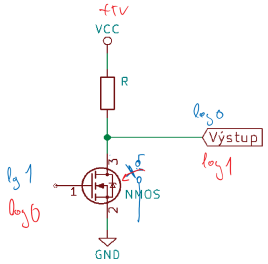
Logické úrovne:
log. 0 = 0.0V až 0.3 * VDD. Ak VDD = 5.0V (0.0 až 1.5V)
log. 1 = 0.7 * VDD až VDD. Ak VDD = 5.0V (3.5 až 5.0V)

- Okrem VDD = 5.0V sa používa aj

VDD = 3.3V a VDD = 2.9V

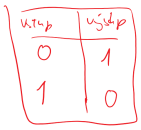
Totem pole



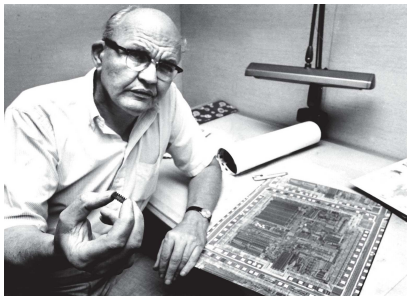


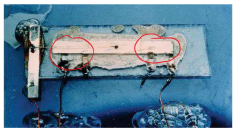
a) Tranzistor zopnutý (1) na výstupe log. 0

b) Tranzistor rozopnutý (0) na výstupe log. 1



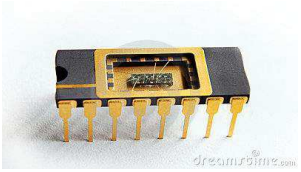
Integrovaný obvod





12. 9. 1958
Americký fyzik Jack Kilby vytvoril prvý integrovaný obvod na jedinom čipe
2000 - Nobel Prize in physics

Integrovaný obvod

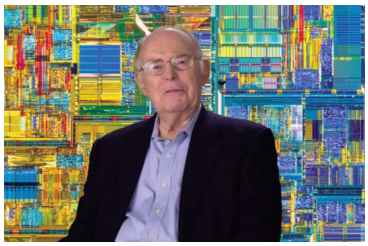


Name	Signification	Year	Transistors number[47]	Logic gates number[48]
SSI	*small-scale integration*	1964	1 to 10	1 to 12
MSI	*medium-scale integration*	1968	10 to 500	13 to 99
LSI	*large-scale integration*	1971	500 to 20,000	100 to 9,999
VLSI	*very large-scale integration*	1980	20,000 to 1,000,000	10,000 to 99,999
ULSI	*ultra-large-scale integration*	1984	1,000,000 and more	100,000 and more

Moorov zákon

Gordon Moore

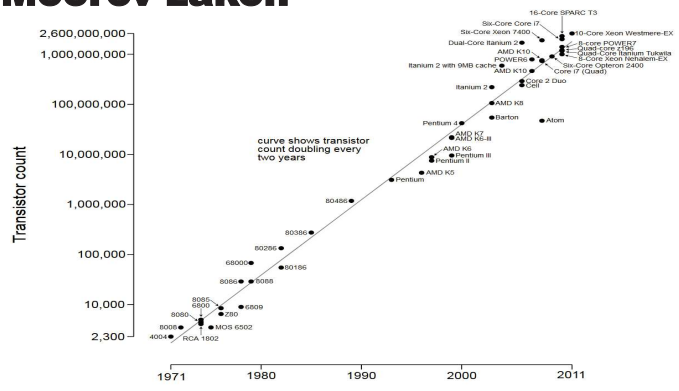
spoluzakladatel firiem Intel
a Fairchild Semiconductor



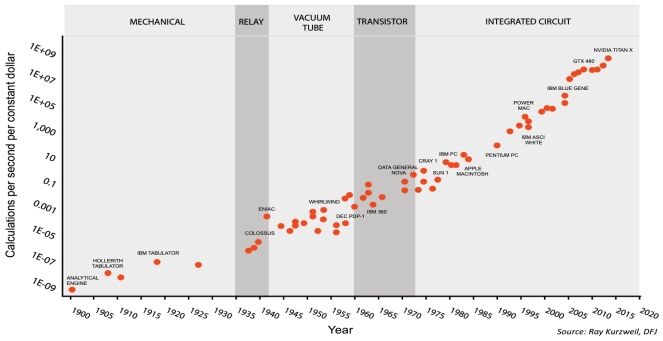
Moore's law is the observation:

The number of transistors in a dense integrated circuit ***doubles*** *approximately every* ***two years*** *(1965)*

Moorov zákon



120 Years of Moore's Law



sli.do
#ZPOC

Ak by sa automobilový priemysel rozvíjal rovnako
ako počítačový, aká by bola rýchlosť dnešných áut?

Moorov zákon

Ak by sa rovnako rozvíjal automobilový priemysel:

300 000 km/h 850 000 km / liter 0,04 $ / ks

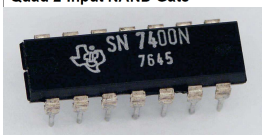
7400

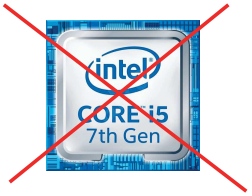
TTL (Transistor-Transistor-Logic)
Integrovaný obvod 4x 2-vst. NAND
Technológia SSI – obsahuje cca **16 tranzistorov** a ďalšie súčiastky
Cena cca 0,30 $ ale bola aj 22$ r. 1965

Nie Intel Core i5-7400 Quad-Core, 3,0 GHz (65 W), TurboBoost 3,5 GHz, Intel HD Graphics 630 (1000 MHz), 6 MB L3 cache, socket 1151, Kaby lake 14 nm
182,- USD **Tranzistorov: 750 000 000**

FAIRCHILD SEMICONDUCTOR

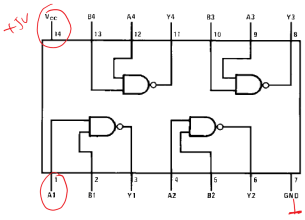
DM74LS00
Quad 2-Input NAND Gate





SN7400

Connection Diagram

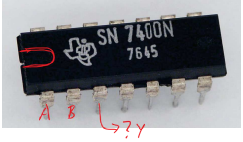


Function Table

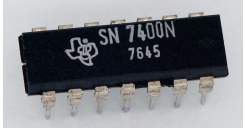
$Y = \overline{AB}$

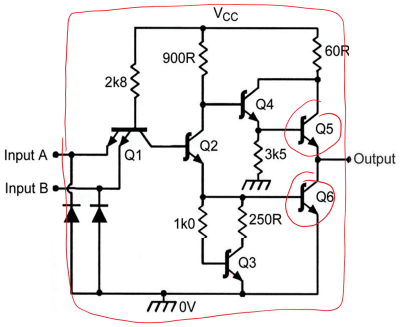
Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level



SN7400





Vnútorné zapojenie jedného NAND hradla

DM74LS00

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

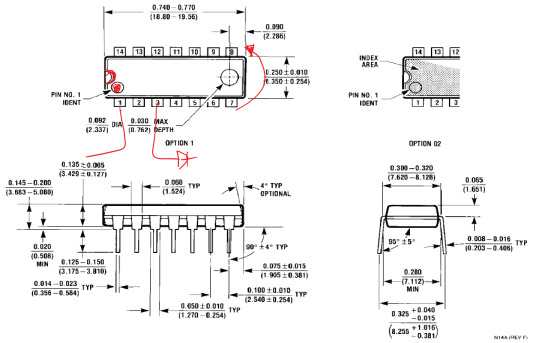
Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		0.8	1.6	mA

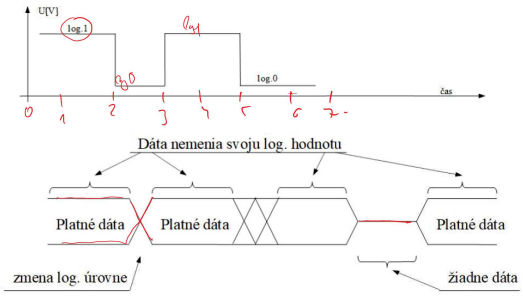
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



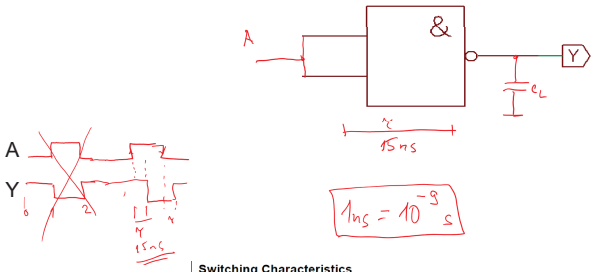
14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

DM74LS00 Quad 2-Input NAND Gate

Časové diagramy



Oneskorenie

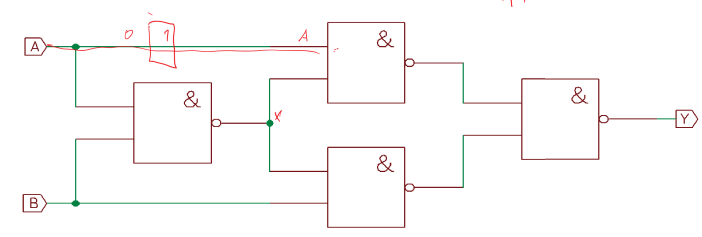


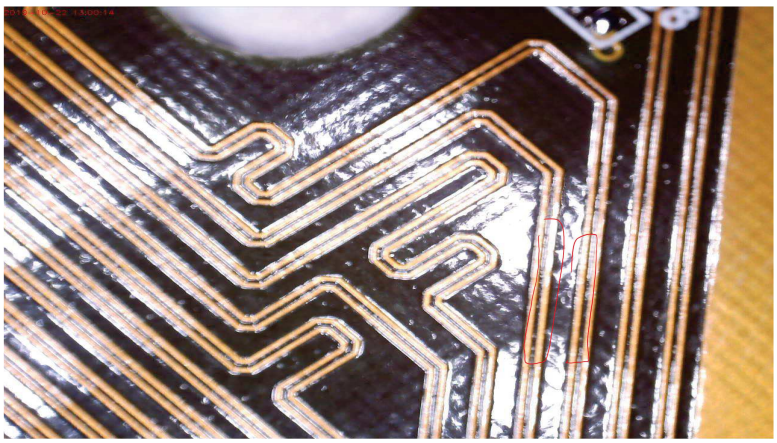
Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

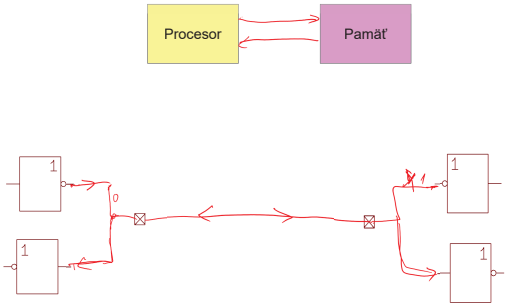
Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF Min	R_L = 2 kΩ, C_L = 15 pF Max	R_L = 2 kΩ, C_L = 50 pF Min	R_L = 2 kΩ, C_L = 50 pF Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	15	ns

Oneskorenie

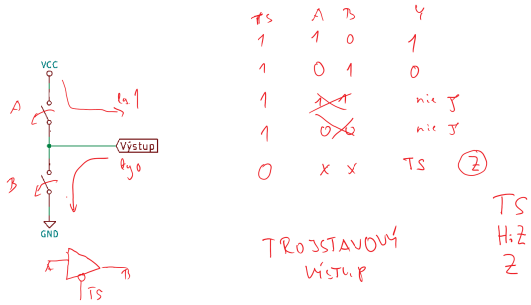




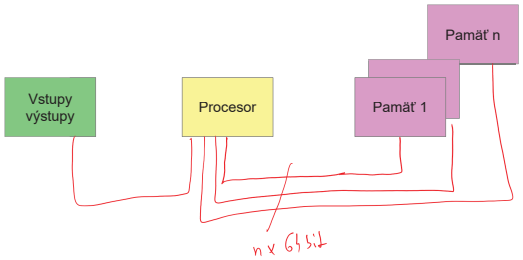
Zbernice – obojsmerný V/V



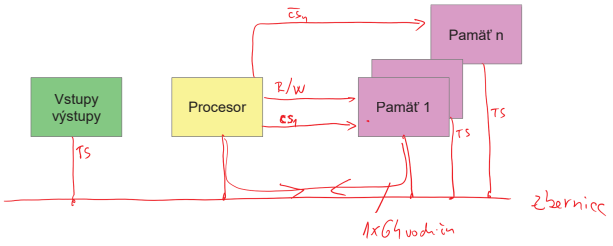
Zbernice – obojsmerný V/V



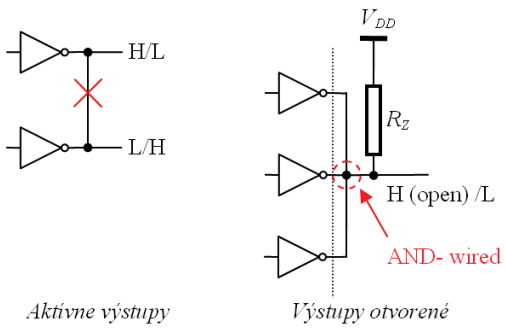
Zbernice – trojstavový výstup



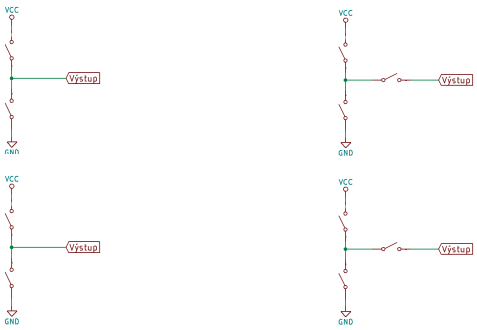
Zbernice – trojstavový výstup



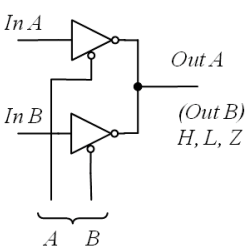
Spájanie vstupov a výstupov

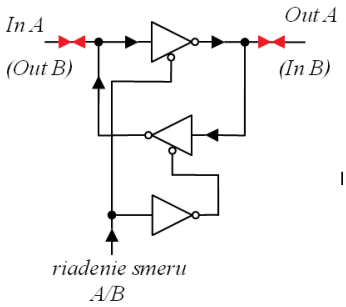


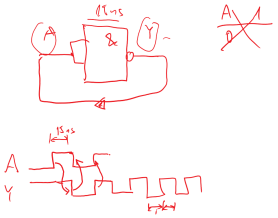
Zbernice – trojstavový výstup

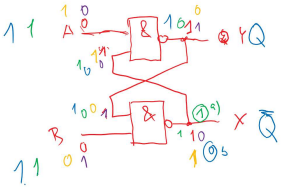


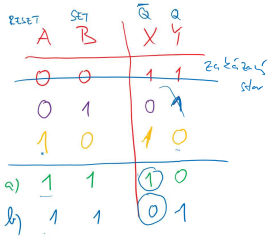
Zbernice

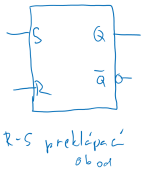












Flip-flop

sli.do #ZPOC

Otázky?

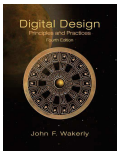
Ohodnoťte dnešnú prednášku, prosím.

Zhrnutie

- Číslicová logika (0,1, De Morganove pravidlá)
- Logické členy (NOT, AND, OR, NAND, NOR, XOR)
- Opis logických obvodov (schéma, tabuľka, rovnica, K-mapa)
- Analýza (schéma, tabuľka, rovnica)
- Syntéza (schéma, tabuľka, rovnica), simulácia a realizácia
- Spínacie prvky (relé, tranzistor, TTL obvody)

Chcem vedieť viac...

John F. WAKERLY:
Digital design.
Stanford University : Prentice Hall, 2006.



Jean-Michel BERNARD, Jean HUGON
a Robert Le Corvec:
Od logických obvodů k mikroprocesorům.
SNTL : Praha, 1982