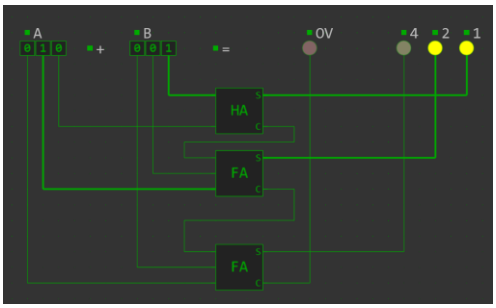
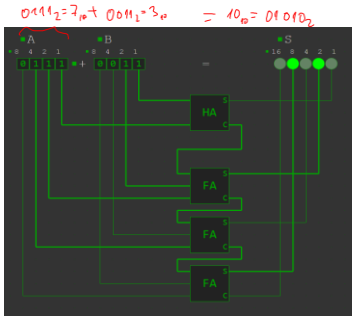


https://simulator.io/board/VuE4wWhzhF/5

1



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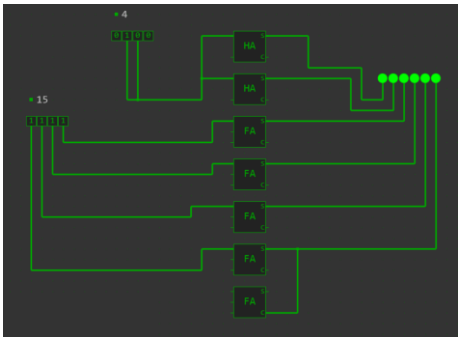

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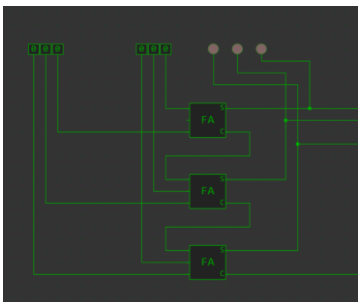

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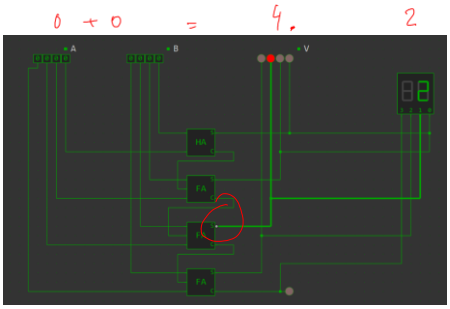
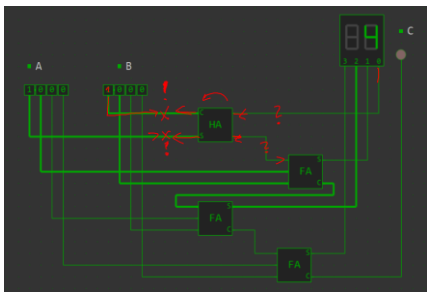


5



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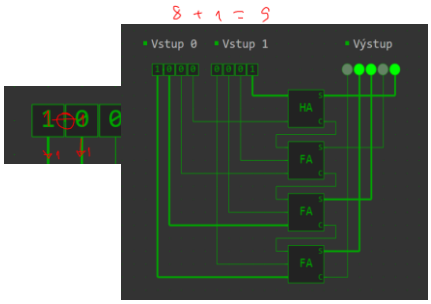
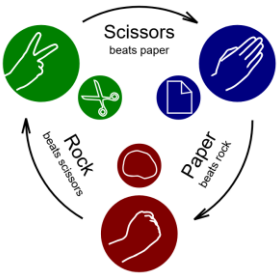
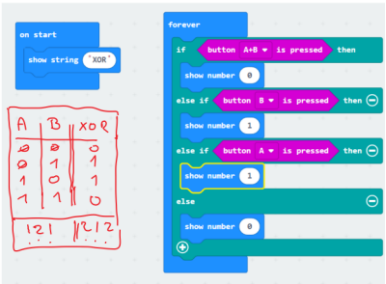

8 + 1 = 9
Vstup 0
Vstup 1
Výstup
HA
FA
FA
FA

7


Scissors
beats paper
Rock
beats scissors
Paper
beats rock

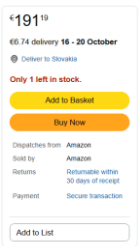
8


on start
show string "XOR"
forever
if button A+B is pressed then
show number 0
else if button B is pressed then
show number 1
else if button A is pressed then
show number 1
else
show number 0

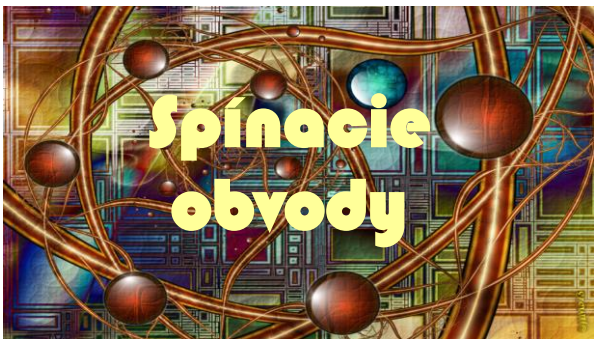
9

10


START GATE
STOP GATE
REACTION TIMER


€191 19
€6.74 delivery 16 - 20 October
Deliver to Slovakia
Only 1 left in stock.
Add to Basket
Buy Now
Dispatches from Amazon
Sold by Amazon
Returns Returnable within 30 days of receipt
Payment Secure transaction
Add to List

11


Spínacie obvody

12

Dnes sa naučíme

- Pochopiť, z čoho staviame logické členy
- Rozdiel medzi mechanickým a elektronickým spínačom
- Ako funguje tranzistor
- Dozvedieť sa ako sa vyrába integrovaný obvod
- Ako je to s rýchlosťou a ako kresliť časové diagramy

13

Spínač

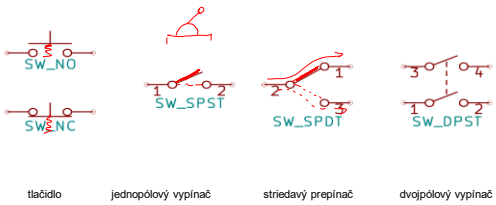
Source: Wikipedia

14

Spínač

NO – Normally Open
NC – Normally Closed
SPST – Single Pole Single Throw
SPDT – Single Pole Double Throw
DPST – Double pole Single Throw

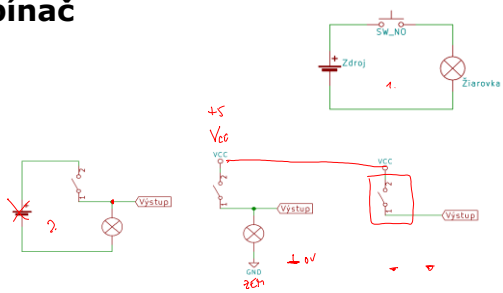
Otvorený v kľudovom stave
Zatvorený v kľudovom stave
Jednopólový vypínač
Striedavý prepínač
Dvojpólový vypínač



tlačidlo | jednopólový vypínač | striedavý prepínač | dvojpólový vypínač

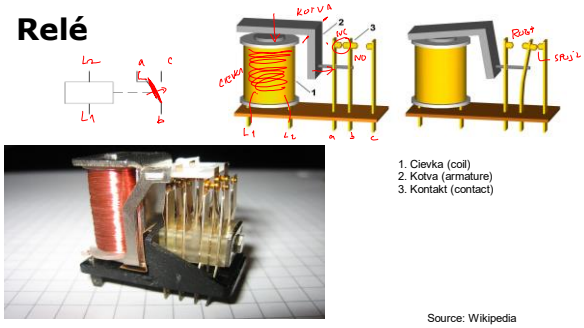
15

Spínač



16

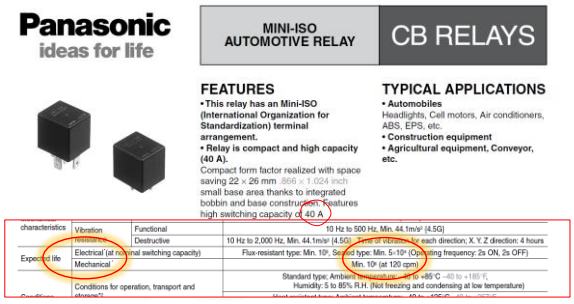
Relé



1. Cievka (coil)
2. Kotva (armature)
3. Kontakt (contact)

Source: Wikipedia

17



18

Claude Elwood Shannon

* 30. apríla 1916, Michigan
† 24. február 2001, Massachusetts

– profesor na MIT

Kybernetika, Teória informácie, Entropia

Symbolická analýza zmeny a spínacie obvody

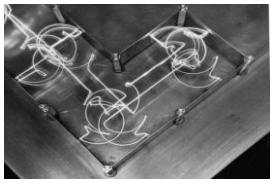
Bell Labs Inc. - reléová logika

Source: Wikipedia, http://cyberneticzoo.com

19

Theseus (1952)

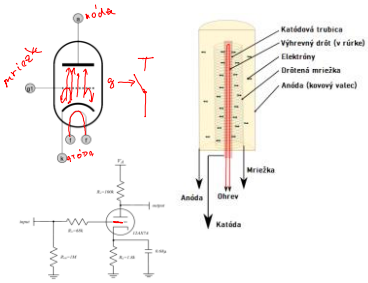
Maze-Solving Mouse



Source: http://cyberneticzoo.com

20

Elektrónka



Source: Wikipedia

21

Elektrónka

ENIAC (1946)

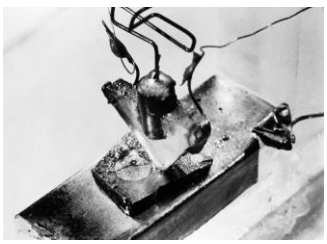
- 17 468 elektrónok
- P =150 kW
- m = 27 000 kg
  2,4 × 0,9 × 30 m
- $487,000
  (ekv. 2016: $6,740,000)

Source: Wikipedia

22

23

Tranzistor



Bell Labs

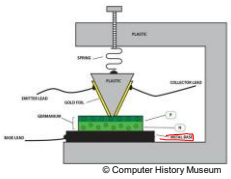
John Bardeen
Walter Brattain
William Shockley

Nobelova cena 1956

Source: Wikipedia

24

Tranzistor



© Computer History Museum

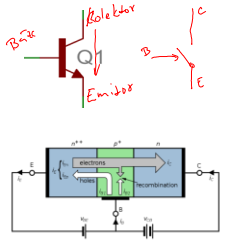
Source: Wikipedia

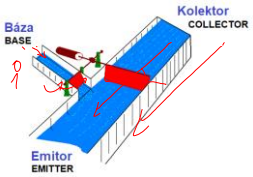
1939: William Shockley (AT&T's Bell Labs) myšlienka náhrady elektrónok
1947: Shockley -> John Bardeen and Walter Brattain prvý reálny tranzistorový zosilňovač
1956: Nobelova cena pre všetkých troch

25

Tranzistor bipolárny, NPN

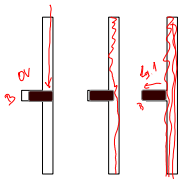
Bipolárny – využíva ako nosiče elektróny aj diery

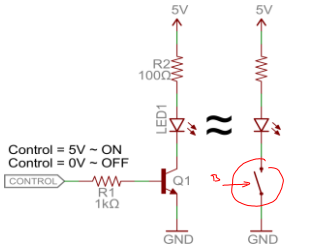




26

Tranzistor



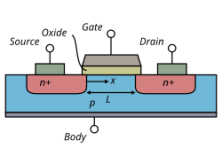


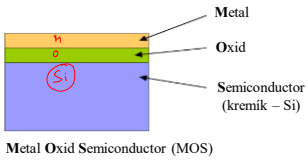
© Sparkfun

27

Poľom riadené tranzistory (unipolárne)

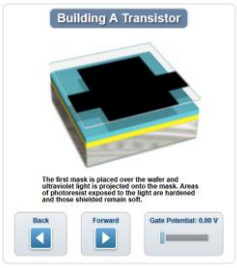
FET – Field Effect Transistor
MOS Metal, Oxid, Semiconductor – technológia
MOSFET – základný typ používaný v integrovaných obvodoch
Nosič náboja je len jeden





Metal Oxid Semiconductor (MOS)

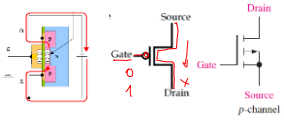
28



https://micro.magnet.fsu.edu/electromag/java/transistor/

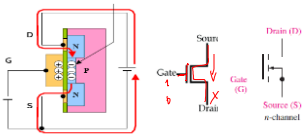
29

Tranzistor PMOS a NMOS (MOS tranzistor s kanálom P a N)



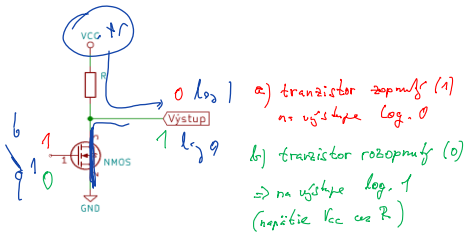
G – gate / hradlo
D – drain / kolektor
S – source / emitor

- historicky najstaršia technológia
- nízka rýchlosť
- zlá zlučiteľnosť s TTL (bipolárnymi) obvodmi



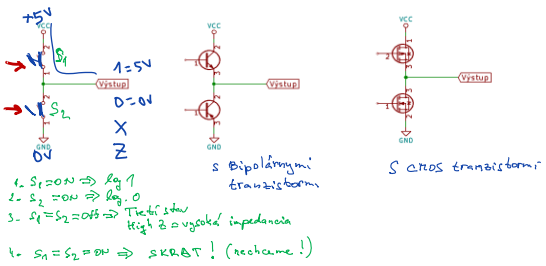
- rýchlosť je vyššia
- zlučiteľné s TTL
- vyššie straty

30



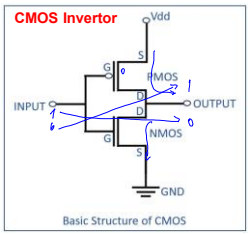
31

Totem pole



32

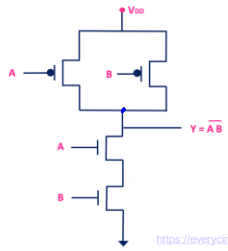
Technológia CMOS (Complentary MOS)



Výhody:
- minimalizované straty
- zlučiteľné s TTL

33

NAND technológiou CMOS



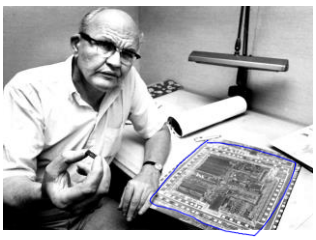
Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

https://everycircuit.com/circuit/5747025316151296/cmos-nand

34

Integrovaný obvod

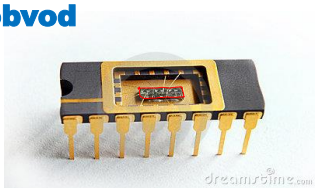


12. 9. 1958
Americký fyzik Jack Kilby vytvoril prvý integrovaný obvod na jedinom čipe @ Texas Instruments

2000 - Nobel Prize in physics

35

Integrovaný obvod



Name	Signification	Year	Transistors number[47]	Logic gates number[48]
SSI	small-scale integration	1964	1 to 10	1 to 12
MSI	medium-scale integration	1968	10 to 500	13 to 99
LSI	large-scale integration	1971	500 to 20,000	100 to 9,999
VLSI	very large-scale integration	1980	20,000 to 1,000,000	10,000 to 99,999
ULSI	ultra-large-scale integration	1984	1,000,000 and more	100,000 and more

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Moorov zákon

Gordon Moore

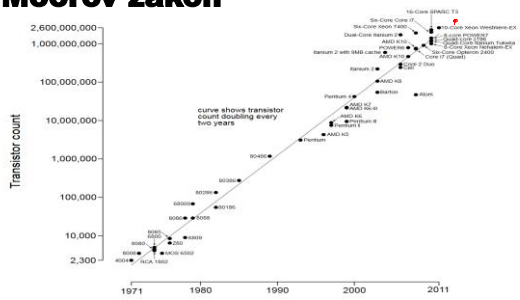
spoluzakladateľ firiem Intel
a Fairchild Semiconductor

Moore's law is the observation:

The number of transistors in a dense integrated circuit ***doubles*** *approximately every* ***two years*** *(1965)*

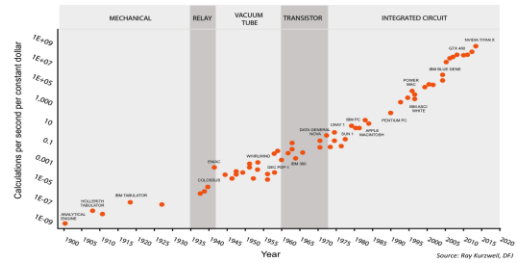
37

Moorov zákon



38

120 Years of Moore's Law



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sli.do
#ZPOC

Ak by sa automobilový priemysel rozvíjal rovnako
ako počítačový, aká by bola rýchlosť dnešných áut?

40

Moorov zákon

Ak by sa rovnako rozvíjal automobilový priemysel:

300 000 km/h

850 000 km / liter

0,04 $ / ks

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7400

TTL (Transistor-Transistor-Logic)
Integrovaný obvod 4x 2-vst. NAND
Technológia SSI – obsahuje cca **16 tranzistorov** a ďalšie súčiastky
Cena cca 0,30 $ ale bola aj 22$ r. 1965

FAIRCHILD
SEMICONDUCTOR

DM74LS00
Quad 2-Input NAND Gate

Nie Intel Core i5-7400 Quad-Core, 3,0 GHz (65 W), TurboBoost 3,5 GHz, Intel HD Graphics 630 (1000 MHz), 6 MB L3 cache, socket 1151, Kaby lake 14 nm 182,- USD **Tranzistorov: 750 000 000**

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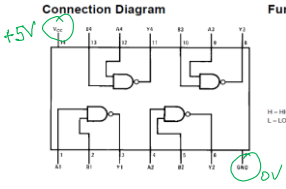
SN7400

Connection Diagram



Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

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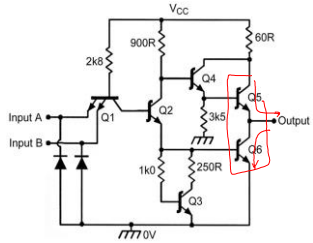
SN7400



https://everycircuit.com/circuit/4806663265714176/ttl-standard-nand-logic-gate

https://www.falstad.com/circuit/index.html

44

DM74LS00

Absolute Maximum Ratings (Note 1)

Supply Voltage 7V
Input Voltage 7V
Operating Free Air Temperature Range 0°C to +70°C
Storage Temperature Range −65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		0.8	1.6	mA

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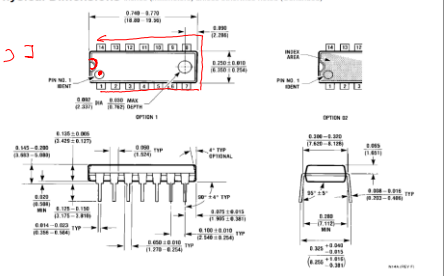
DM74LS00 Quad 2-Input NAND Gate

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

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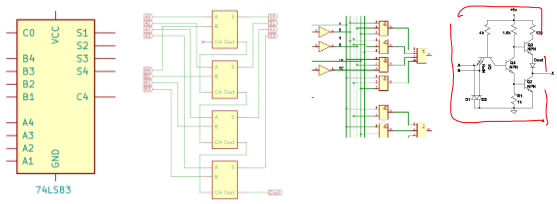
Štvorbitová sčítačka – princíp čiernej skrinky



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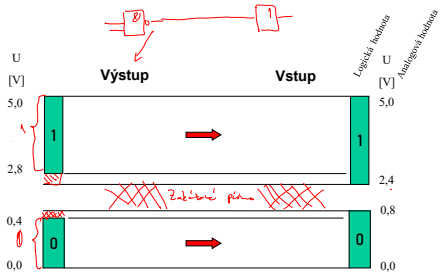
TTL obvody: logické úrovne



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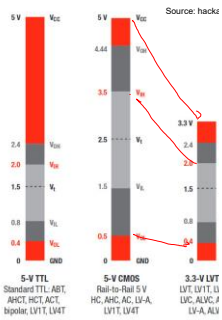
Logické úrovne CMOS

log. 0 = 0,0 až 0,3×V_{DD}
log. 1 = 0,7×V_{DD} až V_{DD}

Ak je V_{DD} = 5,0 V
log. 0 je 0,0 až 1,5V
log. 1 je 3,5 až 5,0V

Okrem 5,0V používa CMOS aj
V_{DD} = 3,3 alebo 1,8 V a pod.



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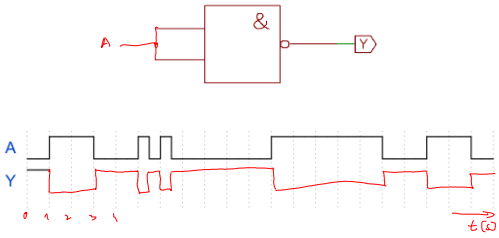
Časové diagramy



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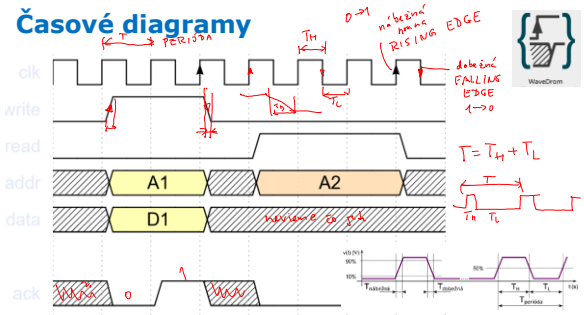
Časové diagramy



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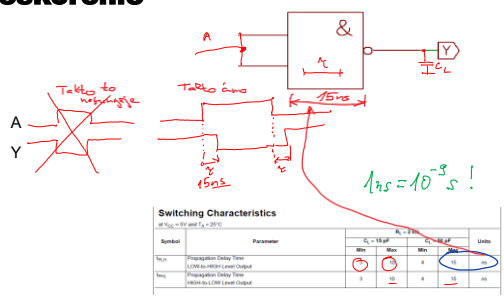
Oneskorenie



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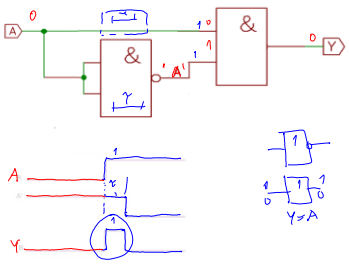
Zákmity / glitch



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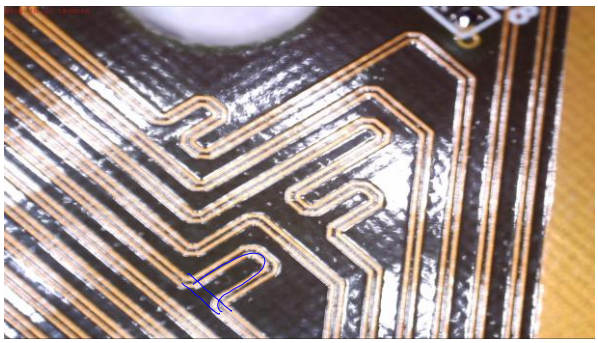

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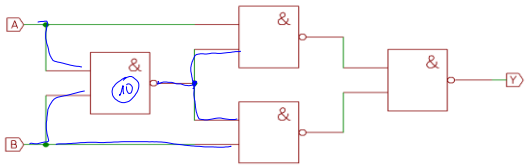
Spájanie vstupov a výstupov



Vstupy: OK

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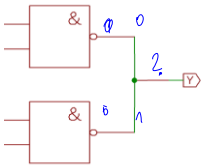
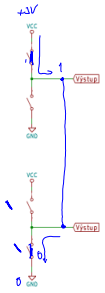
Spájanie výstupov





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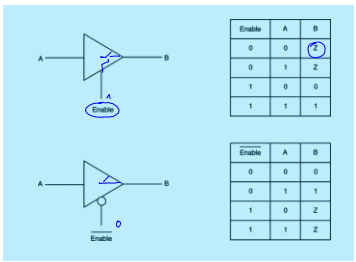
Zbernice – trojstavový výstup

Hi Z



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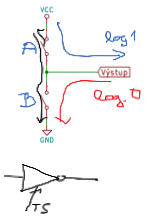
Zbernice – trojstavový výstup



A zapnutý B rozpnutý = log 1

A rozpnutý B zapnutý = log. 0

A aj B rozpnutý = stav vysokej impedancie
High Z
alebo Tretí stav
(obvod je odpojený)

A aj B zapnutý = ~~SKRAT~~ !
nesmie nastať

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sli.do #ZPOC

Ako funguje tranzistor, aké má výhody oproti mechanickému spínaču.

Rozumiem a vedel by som to aj vysvetliť kamošovi	Pochopil som to	Pochopil, ale musím si to ešte pozrieť	Dnes teda nič...
😍	😐	😕	🤯

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Zhrnutie 1-3

- Číslicová logika (0,1, De Morganove pravidlá)
- Logické členy (NOT, AND, OR, NAND, NOR, XOR)
- Opis logických obvodov (schéma, tabuľka, rovnica, K-mapa) časové diagramy
- Analýza (schéma, tabuľka, rovnica)
- Syntéza (schéma, tabuľka, rovnica), simulácia a realizácia
- Spínacie prvky (relé, tranzistor, TTL obvody)

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Chcem vedieť viac...

John F. WAKERLY:
Digital design.
Stanford University : Prentice Hall, 2006.

Jean-Michel BERNARD, Jean HUGON
a Robert Le Corvec:
Od logických obvodů k mikroprocesorům.
SNTL : Praha, 1982

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