Kombinačné logické obvody II

1

Cvičenia: hw knižnica

Možnosť zapožičať na 14 dní

2

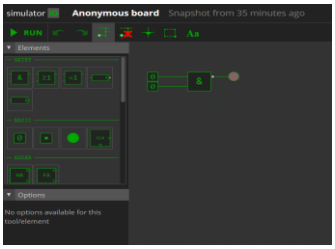
sli.do #ZPOC

NOC VESMÍRU NA FEIKE

17:00 - 22:00

3

Cvičenia: simulator.io



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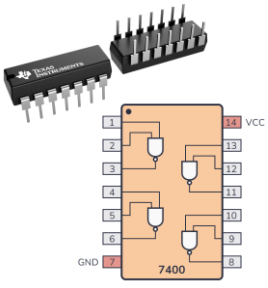
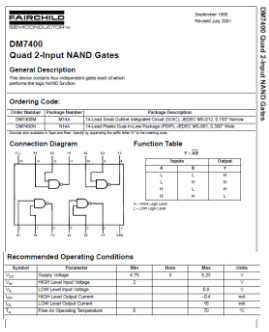
4x dvojvstupový NAND 7400





DM7400
Quad 2-Input NAND Gates

General Description

Ordering Code:

Connection Diagram

Function Table

Recommended Operating Conditions

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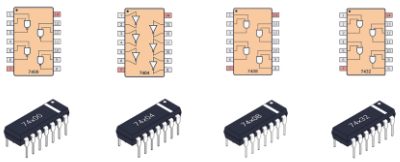
Obvody série 74xx (74xx family)



Prefix	Name	Temperature range	Remarks
54	Military	−55 °C to +125 °C	
64	Industrial	−40 °C to +85 °C	rare
74	Commercial	0 °C to +70 °C	most common
84	Industrial	−25 °C to +85 °C	rare

74	Standard TTL
74H	High-Speed
74L	Low-Power
74F	FAST
74ALS	Advanced Low-Power Schottky
74C	CMOS
74HCT	High-Speed CMOS
74VHCT	Very High-Speed CMOS

https://www.build-electronic-circuits.com/7400-series-integrated-circuits/

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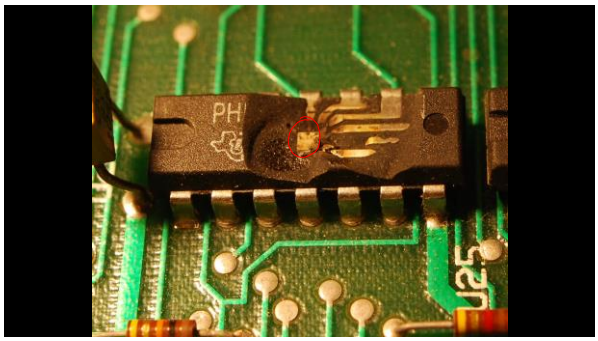

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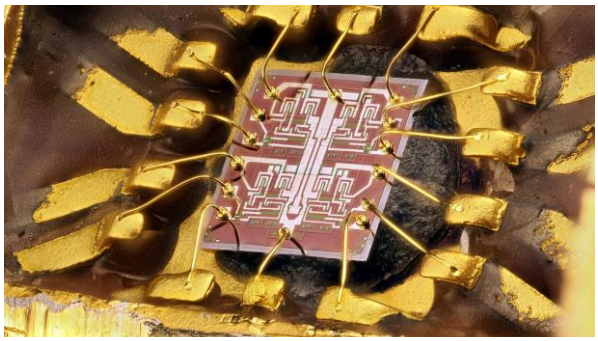

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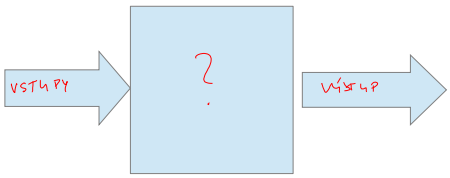
Syntéza logických obvodov



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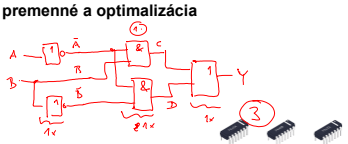
Príklad 1:

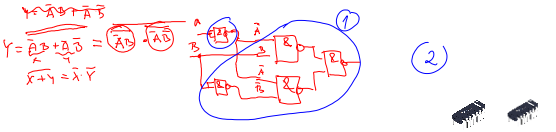
Realizácia obvodu pre 2 premenné a optimalizácia

Zadanie rovnicou

$$Y = \overline{A}.B + \overline{A}.\overline{B}$$



Realizácia len s NAND:



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Maurice Karnaugh

1924 – 2022

Americký fyzik, matematik,

computer scientist a tvorca optimalizačnej metódy pomocou tzv. K-máp

1953 Bell Labs -- dnes:

AT&T

NOKIA BELL LABS

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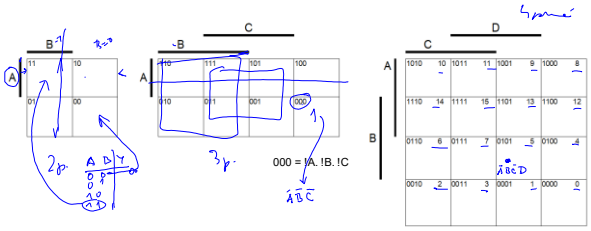
Karnaughove mapy (K-mapy)



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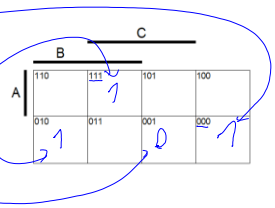
Karnaughove mapy (K-mapy)

	A	B	C	Y
0	0	0	0	1
1	0	0	1	0
2	0	1	0	1
3	0	1	1	0
4	1	0	0	0
5	1	0	1	0
6	1	1	0	0
7	1	1	1	1



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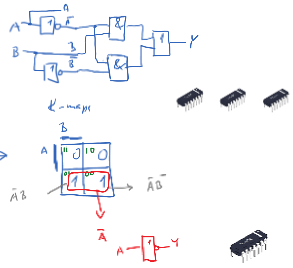
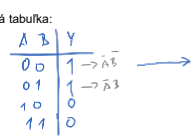
Príklad 1:
Optimalizácia pomocou Karnaughovej mapy pre 2 premenné

Zadanie rovnicou

$Y = \overline{A}.B + \overline{A}.\overline{B}$



Pravdivostná tabuľka:



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Porovnanie podľa AI

Claude

Number of Gates Used	5 gates (2×NOT, 2×AND, 1×OR)	5 NAND gates	1 NAND gate (80% reduction)
Number of IC Chips Required	3 chips (NOT IC, AND IC, OR IC)	2 chips (5 gates = 4 gates/chip) ✓	1 chip (with 3 spare gates) ✓✓
Unused Gates per Design	7 gates wasted (12 total - 5 used)	3 gates spare (8 total - 5 used)	3 gates spare (4 total - 1 used) ✓
Gate Breakdown	• 2 NOT gates • 2 AND gates • 1 OR gate (Mixed logic types)	• 2 NAND inverters ($\overline{A}$, $\overline{B}$) • 2 NAND for AND ops • 1 NAND for OR (All NAND gates)	• 1 NAND inverter ($\overline{A}$)
Logic Levels (Propagation)	3 levels deep	3 levels deep	1 level (66% faster)
Circuit Complexity	Medium (mixed gates)	High (5 gates, but uniform)	Minimal ✓
Power Consumption	High (3 ICs powered, 5 gates active)	Medium (2 ICs powered, 5 gates active)	Lowest (1 IC powered, 1 gate active) ✓✓
PCB Area / Chip Size	Large (3 IC packages)	Medium (2 IC packages) ✓	Minimal (1 IC package) ✓✓
Cost	Highest (3 different IC types to purchase)	Medium (2 identical ICs) ✓	Lowest (1 IC) ✓✓
Reliability	Lower (3 ICs = 3 failure points)	Medium (2 ICs = 2 failure points) ✓	Highest (1 IC = 1 failure point) ✓✓

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Syntéza logických obvodov (Príklad 2)

	A	B	C	Y
0	0	0	0	1
1	0	0	1	0
2	0	1	0	1
3	0	1	1	0
4	1	0	0	0
5	1	0	1	0
6	1	1	0	0
7	1	1	1	1

Minterm je taký logický **súčin (AND)** všetkých premenných, kde každá je buď priamo alebo negovaná, ktorý je **pravdivý len pre jednu konkrétnu kombináciu vstupov**.

Príklad (z tabuľky vedľa):

$A.B.\overline{C}$

Maxterm je logický **súčet (OR)** všetkých premenných, kde každá je buď priamo alebo negovaná, ktorý je **nepravdivý len pre jednu konkrétnu kombináciu vstupov**.

Príklad (z tabuľky vedľa):

1. $(A+B+\overline{C})$
2. $(A+\overline{B}+\overline{C})$

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Syntéza logických obvodov (Príklad 2)

	A	B	C	Y
0	0	0	0	1
1	0	0	1	0
2	0	1	0	1
3	0	1	1	0
4	1	0	0	0
5	1	0	1	0
6	1	1	0	0
7	1	1	1	1

UNDF – úplná normálna disjunktívna forma, alebo tiež súčet súčinov, je logický výraz zapísaný ako **súčet (OR) mintermov,** ktoré obsahujú **všetky** vstupné premenné.

Príklad (z tabuľky vedľa):

$Y = \overline{A}.\overline{B}.\overline{C} + \overline{A}.B.\overline{C} + A.B.C$

UKNF – úplná normálna konjunktívna forma, alebo tiež súčin súčtov, je logický výraz zapísaný ako **súčin (AND) maxtermov,** ktoré obsahujú **všetky** vstupné premenné.

Príklad (z tabuľky vedľa):

$Y = (A+B+\overline{C}).(A+\overline{B}+\overline{C}).(\overline{A}+B+\overline{C}).(\overline{A}+\overline{B}+C).(\overline{A}+\overline{B}+\overline{C})$

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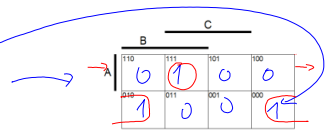
Syntéza logických obvodov (Príklad 2)

	A	B	C	Y
0	0	0	0	1
1	0	0	1	0
2	0	1	0	1
3	0	1	1	0
4	1	0	0	0
5	1	0	1	0
6	1	1	0	0
7	1	1	1	1



$Y = A.B.C + \overline{A}.\overline{C}$

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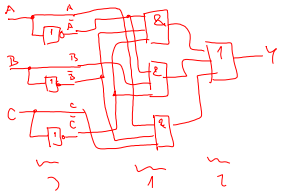
Syntéza logických obvodov (Príklad 2)

	A	B	C	Y
0	0	0	0	1
1	0	0	1	0
2	0	1	0	1
3	0	1	1	0
4	1	0	0	0
5	1	0	1	0
6	1	1	0	0
7	1	1	1	1

$$Y = \bar{A}.\bar{B}.\bar{C} + \bar{A}.B.\bar{C} + A.B.C$$

Schéma zapojenia:



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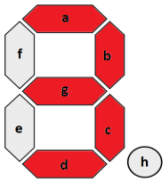
Pr. 4: 7-segmentový dekóder



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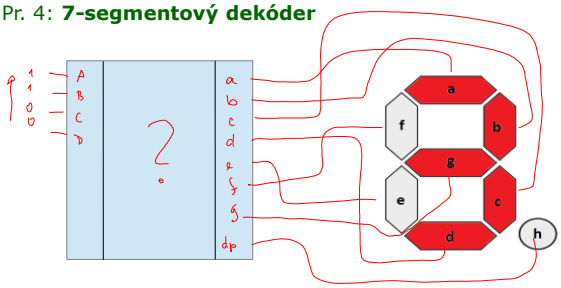
Pr. 4: 7-segmentový dekóder



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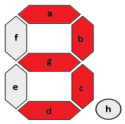
Pr. 4: 7-segmentový dekóder

	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0							
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0							
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0							
5	0	1	0	1							
6	0	1	1	0							
7	0	1	1	1							
8	1	0	0	0							
9	1	0	0	1							



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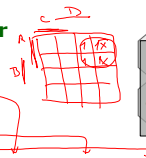
Pr. 4: 7-segmentový dekóder

	A	B	C	D	a
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1



$$a = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}BC\bar{D} + A\bar{B}\bar{C}\bar{D}$$

$$a = (A+B+C+\bar{D})(A+\bar{B}+C+\bar{D})$$

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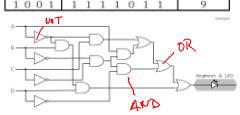
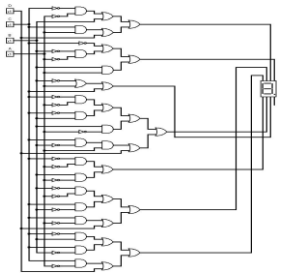
Pr. 4: 7-segmentový dekóder

Binary Inputs	Decoder Outputs	7 Segment Display Outputs
D C B A	a b c d e f g	
0 0 0 0	1 1 1 1 1 1 0	0
0 0 0 1	0 1 1 0 0 0 0	1
0 0 1 0	1 1 0 1 1 0 1	2
0 0 1 1	1 1 1 1 0 0 1	3
0 1 0 0	0 1 1 0 0 1 1	4
0 1 0 1	1 0 1 1 0 1 1	5
0 1 1 0	1 0 1 1 1 1 1	6
0 1 1 1	1 1 1 0 0 0 0	7
1 0 0 0	1 1 1 1 1 1 1	8
1 0 0 1	1 1 1 1 0 1 1	9





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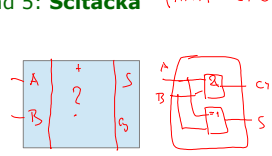
Príklad 5: **Sčítačka** (ARITMETICKÁ ≠ OR)



A	B	S	CY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

(2 bity 1 CARRY)

$CY = A \cdot B$

$S = A \oplus B$

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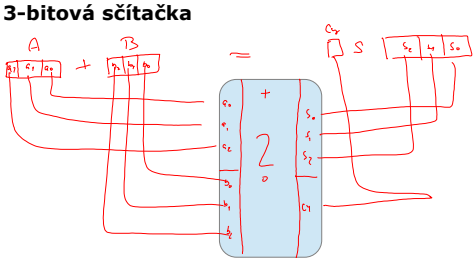
3-bitová sčítačka



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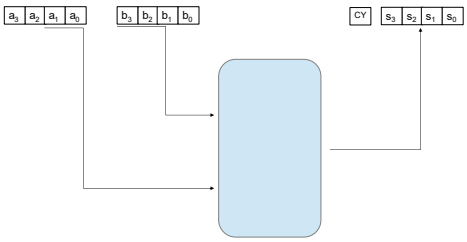
4-bitová sčítačka (cvičenia)



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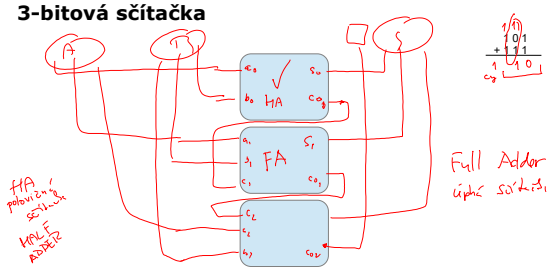
3-bitová sčítačka



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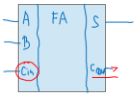
Úplná sčítačka - cvičenia



C_1	A	B	S	C_{2OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

1. $S = \overline{A} \cdot \overline{B} \cdot C_{in} + \overline{A} \cdot B \cdot \overline{C}_{in} + A \cdot \overline{B} \cdot \overline{C}_{in} + A \cdot B \cdot C_{in}$

2. $C_{out} = A \cdot B \cdot C_{in} + \overline{A} \cdot B \cdot C_{in} + A \cdot \overline{B} \cdot C_{in} + A \cdot B \cdot \overline{C}_{in} =$

$C_{out} = B \cdot C_{in} + A \cdot C_{in} + A \cdot B$ ✓

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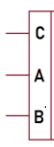
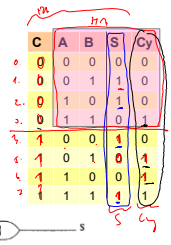
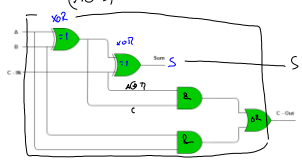
Úplná sčítačka

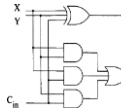
$S = \overline{A} \cdot \overline{B} \cdot C + \overline{A} \cdot B \cdot \overline{C} + A \cdot \overline{B} \cdot \overline{C} + A \cdot B \cdot C =$
$= C (\overline{A} \cdot B + A \cdot \overline{B}) + C (\overline{A \cdot B} + A \cdot B) =$
$= C \oplus (A \oplus B)$

$Cy = \overline{A} \cdot B \cdot C + A \cdot \overline{B} \cdot C + A \cdot B \cdot \overline{C} + A \cdot B \cdot C =$
$= A \cdot B + C \cdot (A \oplus B)$









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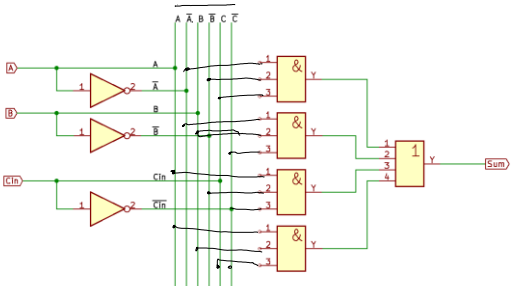
Úplná sčítačka

$$S = \overline{A}\cdot\overline{B}\cdot C_{in} + \overline{A}\cdot B\cdot\overline{C}_{in} + A\cdot\overline{B}\cdot\overline{C}_{in} + A\cdot B\cdot C_{in}$$



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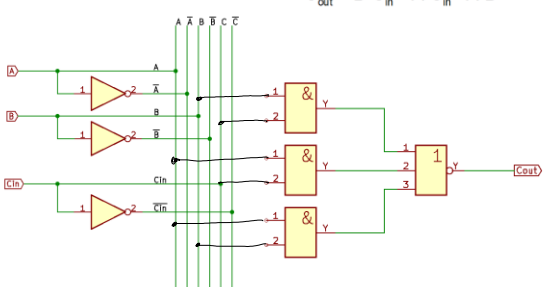
Úplná sčítačka

$$C_{out} = B\cdot C_{in} + A\cdot C_{in} + A\cdot B$$



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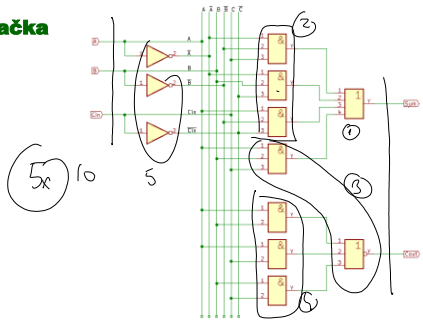
Úplná sčítačka



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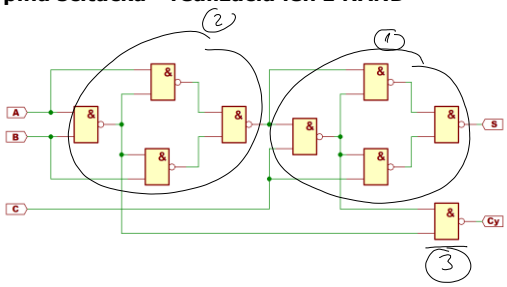
Úplná sčítačka - realizácia len z NAND



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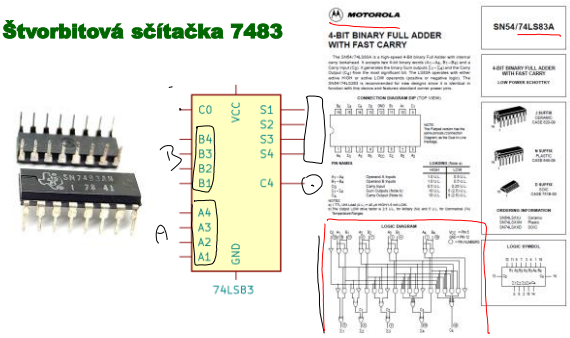
Štvorbitová sčítačka 7483



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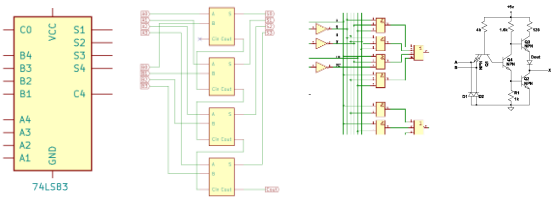
Štvorbitová sčítačka – princíp čiernej skrinky



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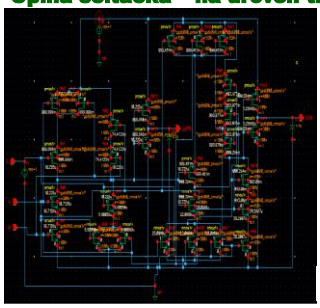
Úplná sčítačka – na úroveň tranzistorov



Amit Bakshi: *Implementation of Power Gating Technique in CMOS Full Adder Cell to Reduce Leakage Power and Ground Bounce Noise for Mobile Application*. International Journal of Electronics, Communication & Instrumentation Engineering Research and Development (IJECERD) ISSN 2249-684X Vol.2, Issue 3 Sep 2012 97-108

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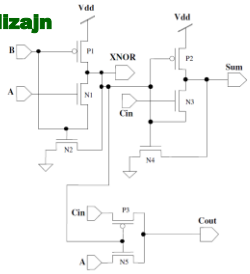
Úplná sčítačka – moderný dizajn



Kumar, M. – Arya, S.K. – Pandey, S.: ***Single bit full adder design using 8 transistors with novel 3 transistors XNOR gate.*** International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.4, December 2011

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Úplná sčítačka – FPGA
Field Programmable Gate Array

```
module add

A3..A0, B3..B0 pin;
S3..S0 pin istype 'out';

A = [0,A3..A0];
B = [0,B3..B0];
S = [S3..S0];

equations
S = A + B;

end add
```

Altera Stratix IV EP4SGX230:
9 200 000 logických hradiel
936 vstupno výstupných blokov
11,5 Mb RAM

Xilinx CPLD:
12 000 logic gates
512 output blocks
3 clock sources

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Zhrnutie

- Prechod medzi zápisom **rovnicou**, **tabuľkou**, **K-mapou** a blokovou **schémou**
- Integrovaný obvod **rodiny 74xx**
- 7-segmentový **dekodér**
- Polovičná a úplná **sčítačka**
- Simulácia logického obvodu

sli.do #ZPOC

Ohodnoťte dnešnú prednášku, prosím.

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Chcem vedieť viac...

John F. WAKERLY:
Digital design.
Stanford University : Prentice Hall, 2006.

Jean-Michel BERNARD, Jean HUGON
a Robert Le Corvec:
Od logických obvodů k mikroprocesorům.
SNTL : Praha, 1982

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