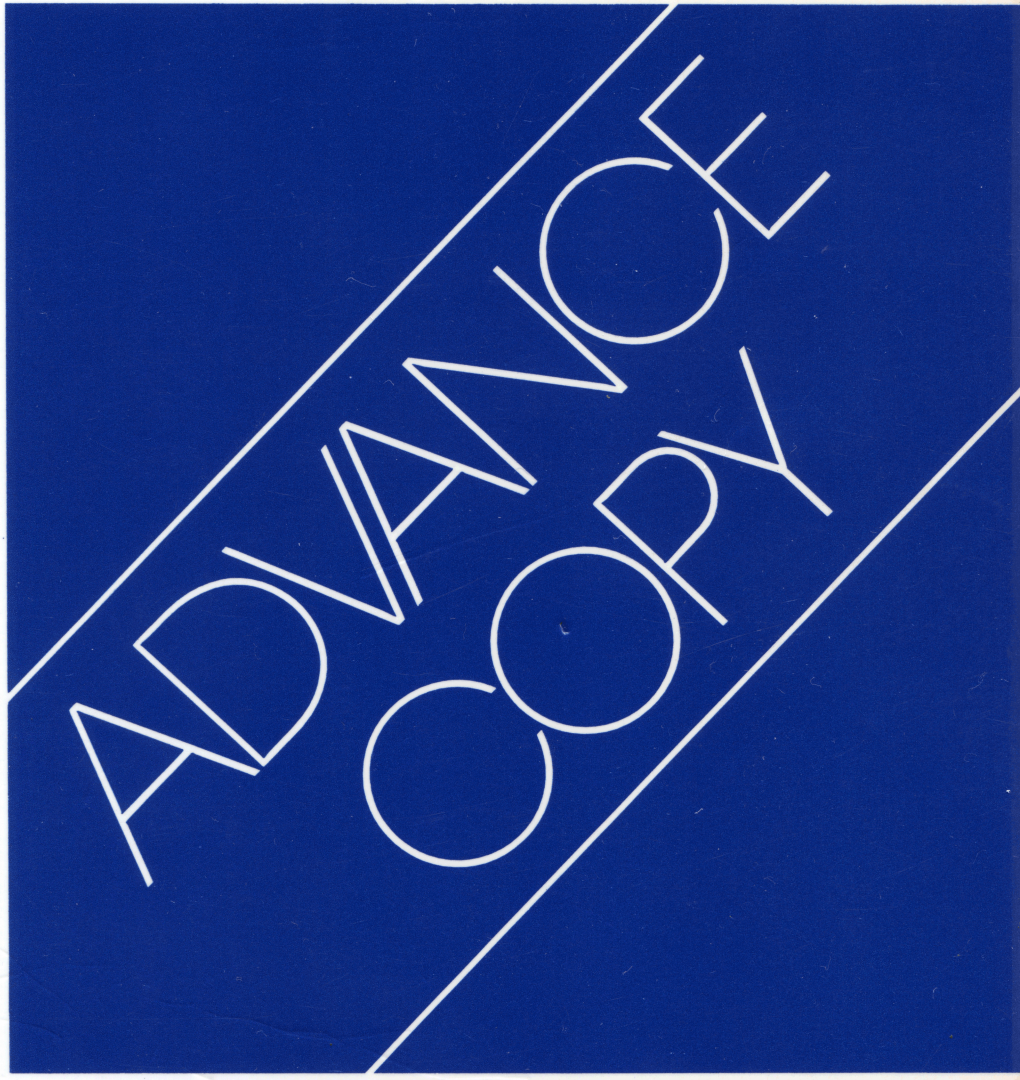
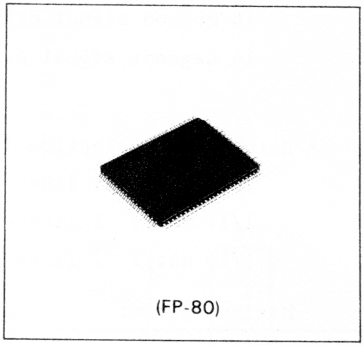
HITACHI LCD DRIVER DATA BOOK



#AP4

HD44780 (LCD-II) (DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER & DRIVER)

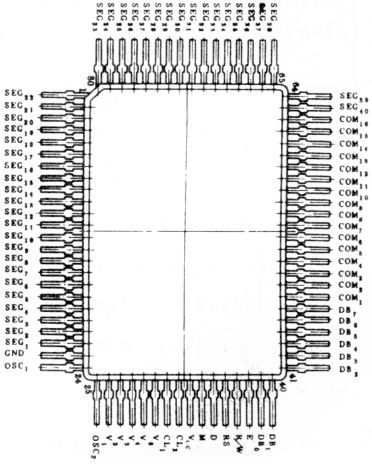


(FP-80)

The LCD-II (HD44780) is a dot matrix liquid crystal display controller & driver LSI that displays alphanumerics, kana characters and symbols. It drives dot matrix liquid crystal display under 4-bit or 8-bit microcomputer or microprocessor control. All the functions required for dot matrix liquid crystal display drive are internally provided on one chip. The user can complete dot matrix liquid crystal display systems with less number of chips by using the LCD-II (HD44780). If a driver LSI HD44100H is externally connected to the HD44780, up to 80 characters can be displayed.

The LCD-II is produced in the CMOS process. Therefore, the combination of the LCD-II with a CMOS microcomputer or microprocessor can accomplish a portable battery-drive device with lower power dissipation.

PIN ARRANGEMENT



(Top View)

FEATURES

- 5 × 7 and 5 × 10 dot matrix liquid crystal display controller driver
- Capable of interfacing to 4-bit or 8-bit MPU.
- Display data RAM ... 80 × 8 bits
  (80 characters, max.)
- Character generator ROM ...
  Character font 5 × 7 dots: 160 characters
  Character font 5 × 10 dobts: 32 characters

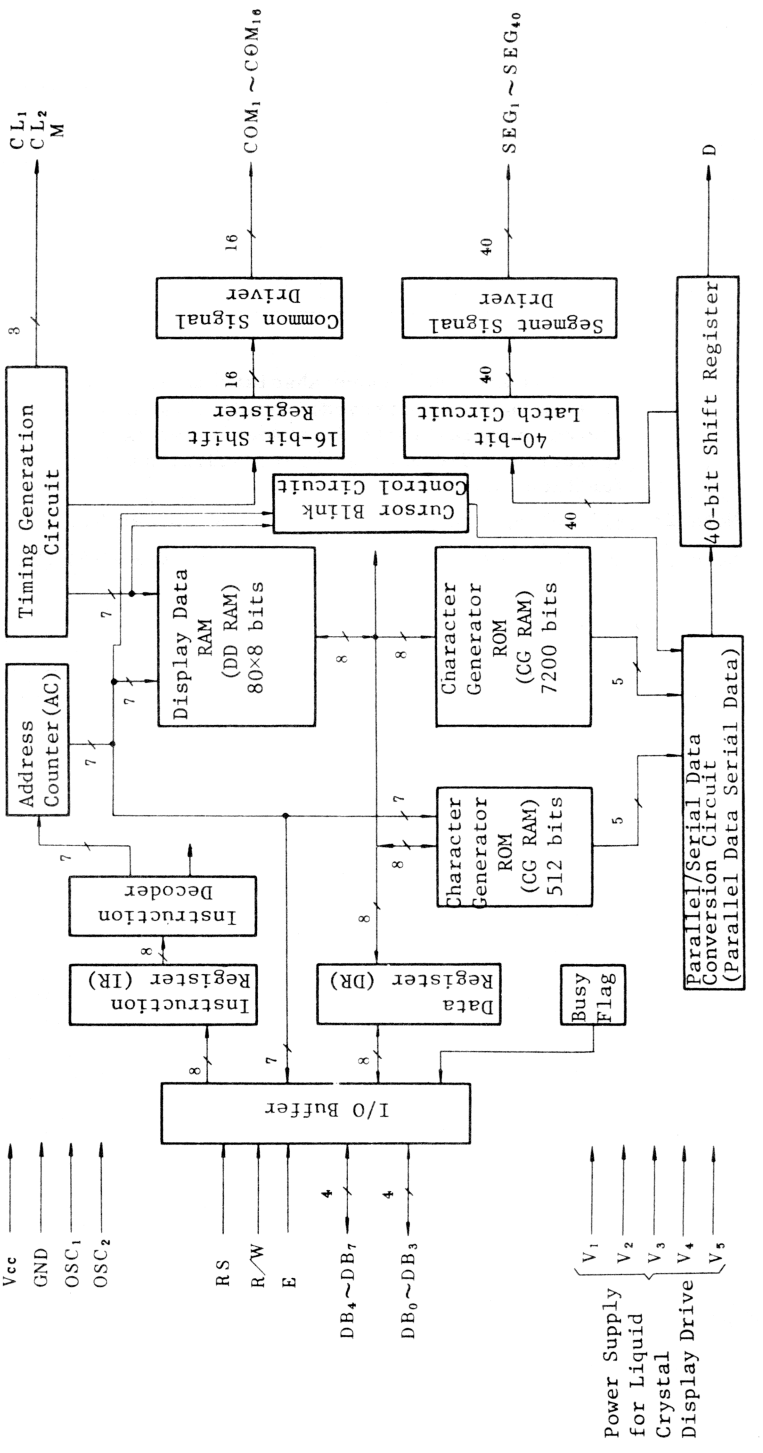
- Both display data and character generator RAMs can be read from the MPU.
- Internal liquid crystal display driver .....
  16 common signal drivers
  14 segment signal drivers (Can be externally extended to 360 segments by liquid crystal display driver HD44100H)
- Duty factor selection (selected by program) .....
  1/8 duty: 1 line of 5 × 7 dots + cursor
  1/11 duty: 1 line of 5 × 10 dots + cursor
  1/16 duty: 2 lines of 5 × 7 dots + cursor

Maximum number of display characters

No. of display lines	Duty factory	Extension	HD44780	HD44100H	No. of display characters
1-line display	1/8 1/11 duty	Not provided	1 pc.	—	8 characters ×1 line
		provided	1 pc.	9 pcs. (8 characters/pc.)	80 characters ×1 line
2-line display	1/16 duty	Not provided	1 pc.	—	8 characters ×2 lines
		provided	1 pc.	4 pcs.(8 characters ×2 lines/pc)	40 characters ×2 lines

- Wide range of instruction functions
  Display clear, Cursor home, Display ON/OFF, Cursor ON/OFF,
  Display character blink, Cursor shift, Display shift
- Internal automatic reset circuit at power ON. (Internal reset circuit)
- Internal oscillation circuit (with external resistor or ceramic filter)
  (External clock operation possible)
- CMOS process
- Logic power supply: A single + 5V (excluding power for liquid crystal display drive)
- Operation temperature range: -20 ~ +75°C
  (Device for -40 ~ +85°C available upon request)
- 80-pin plastic flat package (FP-80)

BLOCK DIAGRAM (HD44780 INTERIOR)



■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Item	Symbol	Limit	Unit	Note
Power Supply Voltage (1)	V_{CC}	-0.3 to +7.0	V	
Power Supply Voltage (2)	V1 to V5	V_{CC}-13.5 to V_{CC}+0.3	V	3
Input Voltage	V_T	-0.3 to V_{CC}+0.3	V	
Operating Temperature	Topr	-20 to +75	°C	
Storage Temperature	Tstg	-55 to +125	°C	

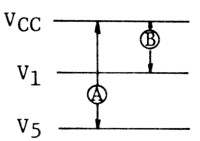
Note 1: If LSI's are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristic limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

Note 2: All voltage values are referenced to GND=0V.

Note 3: Applies to V1 to V5. Must maintain $V_{CC} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$

(high ← → low)

● Electrical Characteristics (V_{CC} = 5V±10%, Ta = -20 to +75°C)



Ⓐ = $V_{CC}-V_5$
Ⓑ = $V_{CC}-V_1$
Ⓐ ≧ 1.5V
Ⓑ ≦ 0.25 ×A

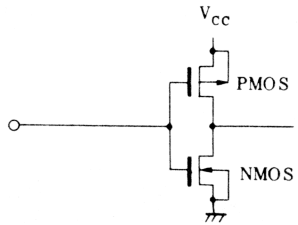
The conditions of V_1, V_5 voltages are for proper operation of the LSI and not for the LCD output level. The LCD drive voltage condition for the LCD output level is specified in "LCD voltage V_{LCD}".

Item	Symbol	Test condition	Limit min	Limit typ	Limit max	Unit	Note
Input "High" Voltage (1)	V_{IH1}		2.2	-	V_{CC}	V	(2)
Input "Low" Voltage (1)	V_{IL1}		-0.3	-	0.6	V	(2)
Output "High" Voltage (1)(TTL)	V_{OH1}	$-I_{OH}$=0.205mA	2.4	-	-	V	(3)
Output "Low" Voltage (1) (TTL)	V_{OL1}	I_{OL}=1.2mA	-	-	0.4	V	(3)
Output "High" Voltage (2)(CMOS)	V_{OH2}	$-I_{OH}$=0.04mA	$0.9V_{CC}$	-	-	V	(4)
Output "Low" Voltage (2) (CMOS)	V_{OL2}	I_{OL}=0.04mA	-	-	$0.1V_{CC}$	V	(4)
Driver Voltage Descending (COM)	V_{COM}	Id=0.05mA	-	-	2.9	V	(10)
Driver Voltage Descending (SEG)	V_{SEG}	Id=0.05mA	-	-	3.8	V	(10)
Input Leakage Current	I_{IL}	V_{in}=0 to V_{CC}	-1	-	1	µA	(5)
Pull up MOS Current	$-I_p$	V_{CC}=5V	50	125	250	µA	
Power Supply Current (1)	I_{CC1}	Ceramic filter oscillation V_{CC}=5V, f_{osc}= 250kHz	-	0.55	0.8	mA	(6)
Power Supply Current (2)	I_{CC2}	Rf oscillation External clock operation V_{CC}=5V, f_{osc}= fcp=270kHz	-	0.35	0.6	mA	(6) (11)
External Clock Operation							
External Clock Frequency	f_{cp}		125	250	350	kHz	(7)
External Clock Duty	Duty		45	50	55	%	(7)
External Clock Rise Time	t_{rcp}		-	-	0.2	µs	(7)
External Clock Fall Time	t_{fcp}		-	-	0.2	µs	(7)
Input "High" Voltage (2)	V_{IH2}		V_{CC}-1.0	-	V_{CC}	V	(12)
Input "Low" Voltage (2)	V_{IL2}		-0.3	-	1.0	V	(12)
Internal Clock Operation (Rf oscillation)							
Clock Oscillation Frequency	f_{osc}	Rf=91kΩ±2%	190	270	350	kHz	(8)
Internal Clock Operation (Ceramic filter oscillation)							
Clock Oscillation Frequency	f_{osc}	Ceramic filter	245	250	255	kHz	(9)
LCD Voltage	V_{LCD1}	V_{CC}-V_5 1/5 bias	4.6	-	11	V	(13)
	V_{LCD2}	V_{CC}-V_5 1/4 bias	3.0	-	11	V	(13)

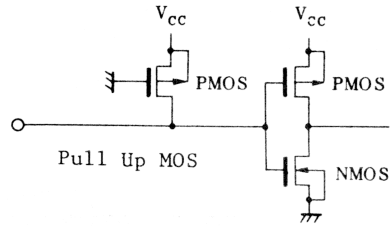
Note 1: The following are I/O terminal configurations except for liquid crystal display output.

- Input Terminal

Applicable Terminals: E (No pull up MOS)

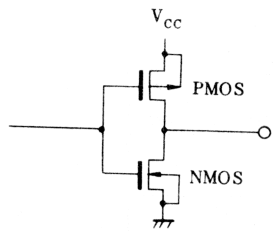


Applicable Terminals: RS, R/W (With pull up MOS)



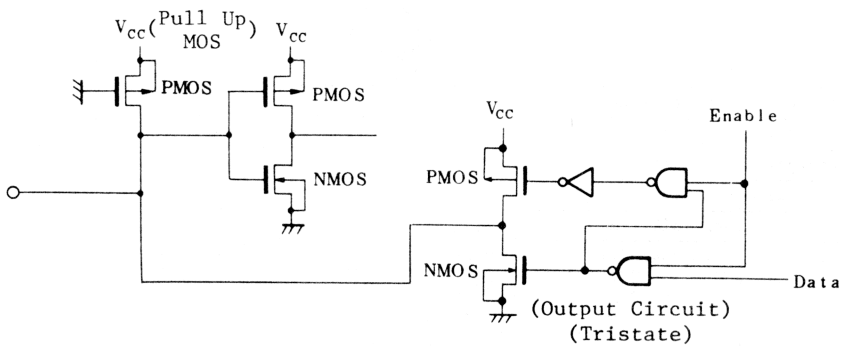
- Output Terminal

Applicable Terminals: CL_1, CL_2, M, D



- I/O Terminal

Applicable Terminals: DB_0 to DB_7



Note 2: Input terminals and I/O terminals. Excludes OSC_1 terminals.

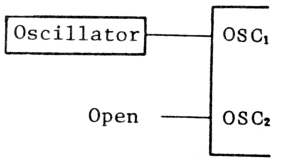
Note 3: I/O terminals.

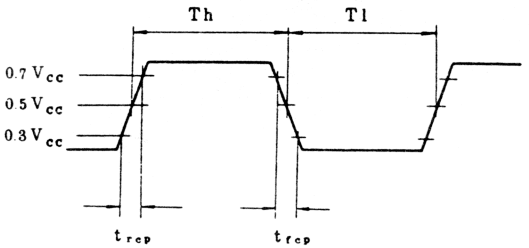
Note 4: Output terminals.

Note 5: Current flowing through pull-up MOS's and output drive MOS's is excluded.

Note 6: Input/Output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.

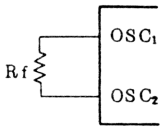
Note 7: External clock operation.





$$\text{Duty} = \frac{Th}{Th + Tl} \times 100\%$$

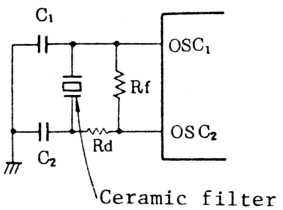
Note 8: Internal oscillator operation using oscillation resistor Rf.



Rf : 91kΩ± 2 %

Since oscillation frequency varies depending on OSC_1 and OSC_2 terminal capacity, wiring length for these terminals should be minimized.

Note 9: Internal oscillator operation using a ceramic filter.is used.



Ceramic filter: CSB250A (Murata)

Rf: 1MΩ ±10%

C_1: 680pF±10%

C_2: 680pF±10%

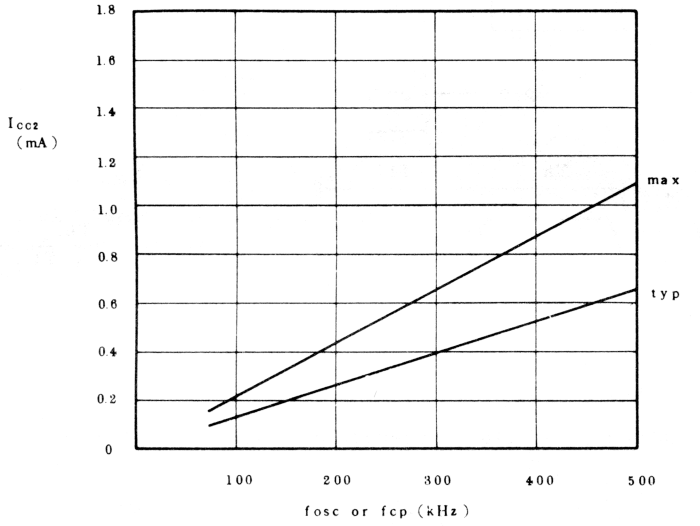
Rd: 3.3kΩ±5%

Note 10: Applies to both V_{COM} and V_{SEG} voltage drops.

V_{COM}: From poer supply terminal V_{CC}, V_1, V_4, V_5 to each common signal terminal (COM_1 to COM_{16})

V_{SEG}: From power supply terminal V_{CC}, V_2, V_3, V_5 to each segment signal terminal (SEG_1 to SEG_{40})

Note 11: Relation between operation frequency and current consumption is shown in this diagram. (V_{CC} = 5V)



Note 12: Applied to OSC_1 terminal.

Note 13: The condition for COM pin voltage drop (V_{COM}) and SEG pin voltage drop (V_{SEG}).

● Timing Characteristics

Write Operation

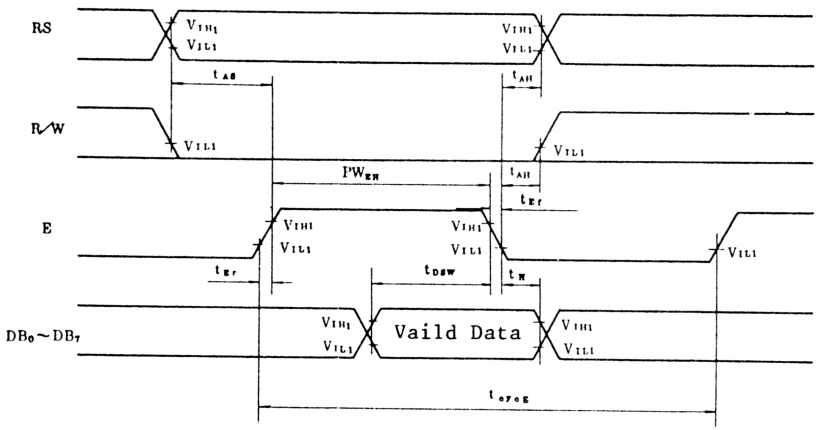


Fig. 1 Bus Write Operation Sequence
(Writing data from MPU to HD44780)

Read Operation

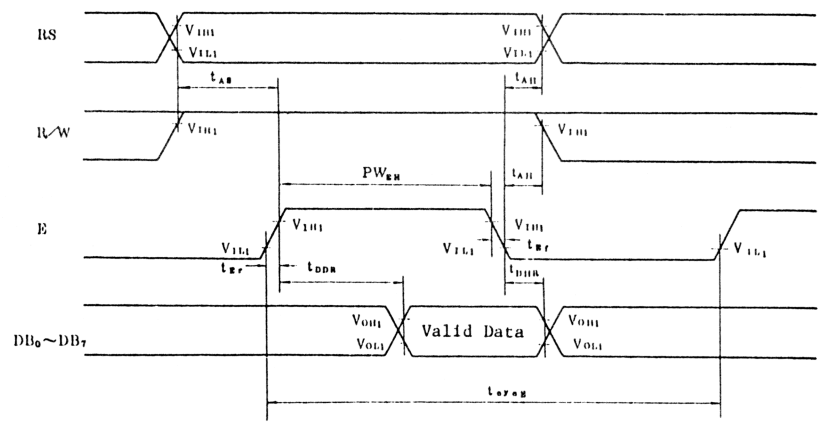


Fig. 2 Bus Read Operation Sequence
(Reading out data from HD44780 to MPU)

Interface Signal with Driver LSI HD44100H

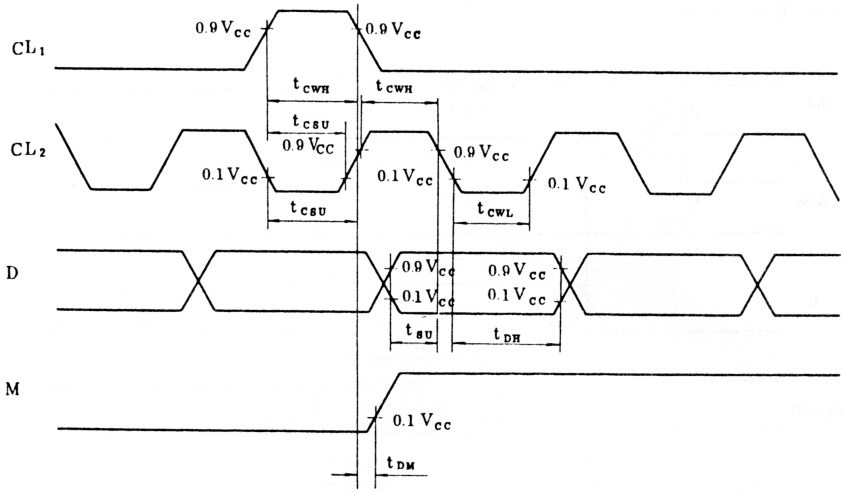


Fig. 3 Sending Data to Driver LSI HD44100H

● Bus Timing Characteristics (V_{CC} = 5.0V ± 10%, GND = 0V, Ta = -20 to +75°C)

Write Operation (Writing data from MPU to HD44780)

Item		Symbol	Test condition	Limit		Unit
				min	max	
Enable Cycle Time		$t_{cyc}E$	Fig. 1	1000	-	ns
Enable Pulse Width	"High" level	PW_{EH}	Fig. 1	450	-	ns
Enable Rise/Fall Time		t_{Er}, t_{Ef}	Fig. 1	-	25	ns
Address Set-up Time	RS, R/W —E	t_{AS}	Fig. 1	140	-	ns
Address Hold Time		t_{AH}	Fig. 1	10	-	ns
Data Set-up Time		t_{DSW}	Fig. 1	195	-	ns
Data Hold Time		t_H	Fig. 1	10	-	ns

Read Operation (Reading data from HD44780 to MPU)

Item		Symbol	Test condition	Limit		Unit
				min	max	
Enable Cycle Time		$t_{cyc}E$	Fig. 2	1000	-	ns
Enable Pulse Width	"High" level	PW_{EH}	Fig. 2	450	-	ns
Enable Rise/Fall Time		t_{Er}, T_{Ef}	Fig. 2	-	25	ns
Address Set-up Time	RS, R/W —E	t_{AS}	Fig. 2	140	-	ns
Address Hold Time		t_{AH}	Fig. 2	10	-	ns
Data Delay Time		t_{DDR}	Fig. 2	-	320	ns
Data Hold Time		t_{DHR}	Fig. 2	20	-	ns

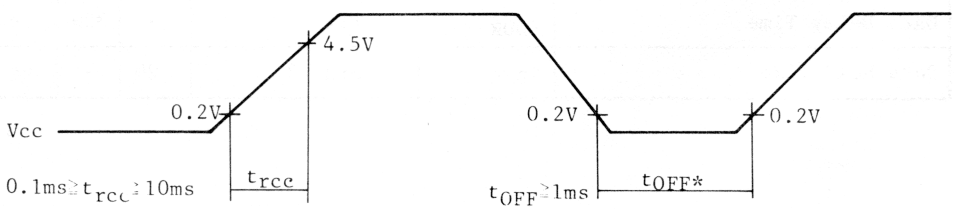
● Interface Signal with HD44100H Timing Characteristics
(V_{CC} = 5.0V ± 10%, GND = 0V, Ta = -20 to +75°C)

Item		Symbol	Test condition	Limit		Unit
				min	max	
Clock Pulse Width	"High" level	t_{CWH}	Fig. 3	800	-	ns
Clock Pulse Width	"High" level	t_{CWL}	Fig. 3	800	-	ns
Clock Set-up Time		t_{CSU}	Fig. 3	500	-	ns
Data Set-up Time		t_{SU}	Fig. 3	300	-	ns
Data Hold Time		t_{DH}	Fig. 3	300	-	ns
M Delay Time		t_{DM}	Fig. 3	-1000	1000	ns

● Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Test condition	Limit		Unit
			min	max	
Power Supply Rise Time	trcc	-	0.1	10	ns
Power Supply OFF Time	t_{OFF}	-	1	-	ns

Since the internal reset circuit will not operate normally unless the preceding conditions are met, initialize by instruction.
(Refer to "Initializing by Instruction")



(Note) t_{OFF} stipulates the time of power OFF for power supply instantaneous dip or when power supply repeats ON and OFF.

■ Terminal Function

Table 1 Functional Description of Terminals

Signal name	No. of lines	Input/ Output	Connected to	Function
RS	1	Input	MPU	Signal to select registers "0": Instruction register (for write) Busy flag; address counter (for read) "1": Data register (for read and write)
R/W	1	Input	MPU	Signal to select read (R) and write (W) "0": Write "1": Read
E	1	Input	MPU	Operation start signal for data read/ write
DB_4 ~ DB_7	4	Input/ Output	MPU	Higher order 4 lines data bus with bidirectional three-state. Used for data transfer between the MPU and the HD44780. DB_7 can be used as a BUSY flag.
DB_0 ~ DB_3	4	Input/ Output	MPU	Lower order 4 lines data bus with bidirectional three-state. Used for data transfer between the MPU and the HD44780. These four are not used during 4-bit operation.
CL_1	1	Output	HD44100H	Clock to latch serial data D sent to the driver LSI HD44100H.
CL_2	1	Output	HD44100H	Clock to shift serial data D.
M	1	Output	HD44100H	Switch signal to convert liquid crystal drive waveform to AC.
D	1	Output	HD44100H	Character pattern data corresponding to each common signal is serially sent. "0": Non selection "1": Selection
COM_1 ~ COM_{16}	16	Output	Liquid crystal display	Common signals that are not used are charged to non-selection waveforms. That is, COM_9 ~ COM_{16} are in non-selection waveform at 1/8 duty factor, and COM_{12} ~ COM_{16} are in non-selection waveform at 1/11 duty factor.
SEG_1 ~ SEG_{40}	40	Output	Liquid crystal display	Segment signal
V_1 ~ V_5	5		Power supply	Power supply for liquid crystal display drive
V_{CC}, GND	2		Power supply	V_{CC}; +5V, GND; 0V
OSC_1, OSC_2	2			Terminals connected to resister or ceramic filter for internal clock osillation. For external clock operation, the clock is input to OSC_1.

FUNCTION OF EACH BLOCK

(1) Register

The HD44780 has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written from the MPU but not read by the MPU.

The DR temporarily stores data to be written into the DD RAM or the CG RAM and data to be read out from DD RAM or CG RAM. Data written into the DR from the MRU is automatically written into the DD RAM or the CG RAM by internal operation. The DR is also used for data storage when reading data from the DD RAM or the CG RAM. When address information is written into the IR, data is read into the DR from the DD RAM or the CG RAM by internal operation. Data transfer to the MPU is then completed by the MPU reading DR. After the MPU reads the DR, data in the DD RAM or CG RAM at the next address is sent to the DR for the next read from the MPU. Register selector (RS) signals make their selection from these two registers.

Table 2 Register Selection

RS	R/W	Operation
0	0	IR write as internal operation (Display clear, etc.)
0	1	Read busy flag (DB_7) and address counter (DB_0 ~ DB_6)
1	0	DR write as internal operation (DR to DD or CG RAM)
1	1	DR read as internal operation (DD or CG RAM to DR)

(2) Busy flag (BF)

When the busy flag is "1", the HD44780 is in the internal operation mode, and the next instruction will not be accepted. As Table 2 shows, the busy flag is output to DB_7 when RS=0 and R/W=1. The next instruction must be written after ensuring that the busy flag is "0".

(3) Address counter (AC)

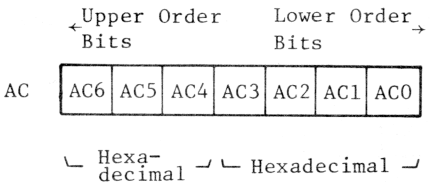
The address counter (AC) assigns addresses to DD and CG RAMs. When an instruction for address is written in IR, the address information is sent from IR to AC. Selection of either DD or CG RAM is also determined concurrently by the instruction.

After writing into (or reading from) DD or CG RAM display data, AC is automatically incremented by +1 (or decremented by -1). AC contents are output to DB_0 ~ DB_6 when RS=0 and R/W=1, as shown in Table 2.

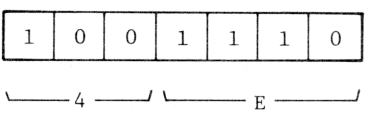
(4) Display data RAM (DD RAM)

The display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80×8 bits, or 80 characters. The display data RAM (DD RAM) that is not used for display can be used as a general data RAM. Relations between DD RAM addresses and positions on the liquid crystal display are shown below.

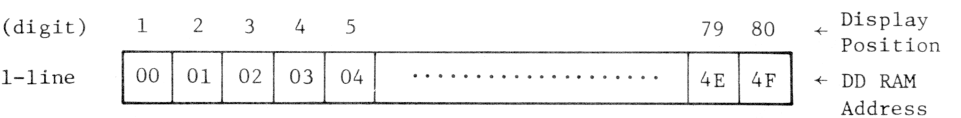
The DD RAM address (A_{DD}) is set in the Address Counter (AC) and is represented in hexadecimal.



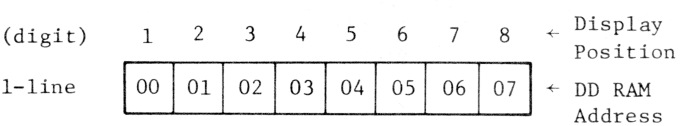
(Example) DD RAM address "4E"



1-line Display (N=0)



(a) When the display characters are less than 80, the display begins at the head position. For example, 8 characters using 1 HD44780 are displayed as:



When the display shift operation is performed, the DD RAM address moves as:

(Left Shift Display)	01	02	03	04	05	06	07	08
(Right Shift Display)	4F	00	01	02	03	04	05	06

(b) 16-character display using an HD44780 and an HD44100H is as shown below:

(digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM Address

HD44780 Display — HD44100H Display

When the display shift operation is performed, the DD RAM address moves as:

(Left Shift Display	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
(Right Shift Display)	4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E

(c) The relation between display position and DD RAM address when the number of display digits is increased through the use of one HD44780 and two or more HD44100H's can be considered an extension of (b).

Since the increase can be 8 digits for each additional HD44100H, up to 80 digits can be displayed by externally connecting 9 HD44100H's.

(digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	...	73	74	75	76	77	78	79	80	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	----	48	49	4A	4B	4C	4D	4E	4F	← DD RAM Address

HD44780 Diaplay — HD44100H(1) Display — HD44100H (2)∿(8) Display — HD44100H(9) Display

2-line Display (N=1)

(digit)	1	2	3	4	5	...	39	40	← Display Position
1-line	00	01	02	03	04	.....	26	27	← DD RAM Address
2-line	40	41	42	43	44	.....	66	67	

(a) When the number of display characters is less than 40 × 2 lines, the 2 lines from the head are displayed. Note that the first line end address and the second line start address are not consecutive. For example, when an HD44780 is used, 8 characters × 2 lines are displayed as:

(digit)	1	2	3	4	5	6	7	8	← Display Position
1-line	00	01	02	03	04	05	06	07	← DD RAM Address
2-line	40	41	42	43	44	45	46	47	

When display shift is performed, the DD RAM address moves as:

(Left Shift Display)	01	02	03	04	05	06	07	08
	41	42	43	44	45	46	47	48

(Right Shift Display)	27	00	01	02	03	04	05	06
	67	40	41	42	43	44	45	46

(b) 16 characters × 2 lines are displayed when an HD44780 and an HD44100H are used.

(digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM Address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

└── HD44780 Display ──┘└── HD44100H Display ──┘

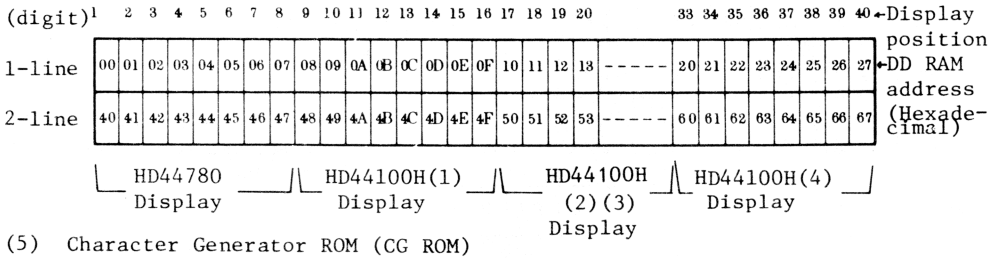
When display shift is performed, the DD RAM address moves as follows:

(Left Shift Display)	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50

(Right Shift Display)	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

(c) The relation between display position and DD RAM address when the number of display digits is increased by using one HD44780 and two or more HD44100H's, can be considered an extension of (b).

Since the increase can be 8 digits × 2 lines for each additional HD44100H, up to 40 digits 2 lines can be displayed by connecting 4 HD44780's externally.



(5) Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 7 dot or 5 × 10 dot character patterns from 8-bit character codes. It can generate 160 types of 5 × 7 dot character patterns and 32 types of 5 × 10 dot character patterns. Table 3 and 4 show the relation between character codes and character patterns in the Hitachi standard HD44780A00. User defined character patterns are also available by mask-programming ROM. For details, see "The LCD-II (HD44780) Breadboard User's Manual".

(6) Character Generator RAM (CG RAM)

The character generator RAM is the RAM with which the user can rewrite character patterns by program. With 5 × 7 dots, 8 byptes of character patterns can be written and with 5 × 10 dots 4 types can be written. Write the character codes in the left columns of Tables 3 and 4 to display character patterns stored in CG RAM.

Table 5 shows the relation between CG RAM addresses and data and display patterns.

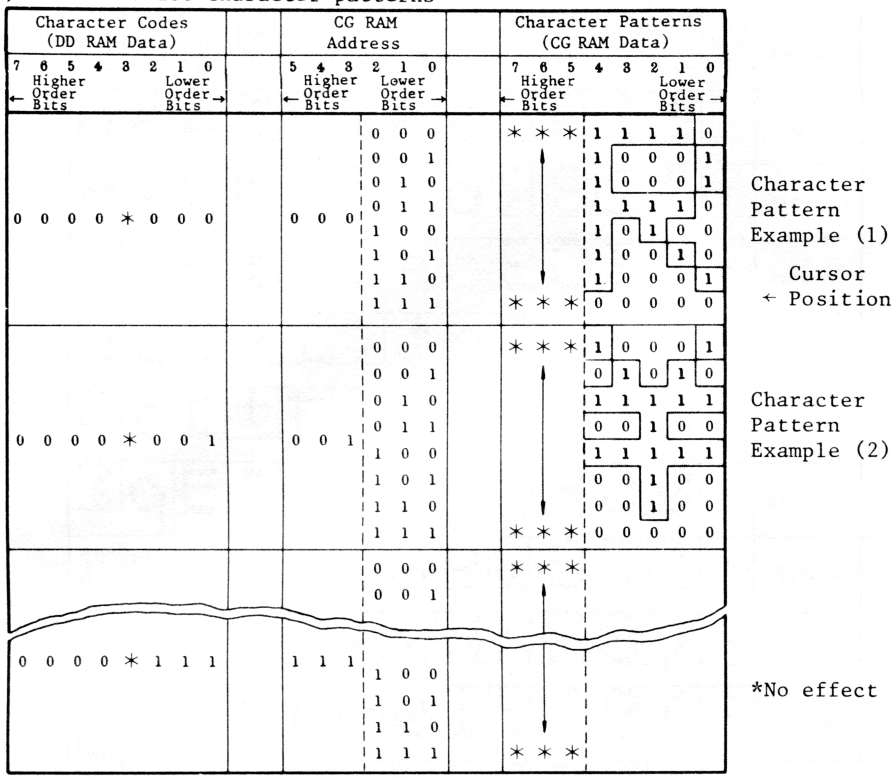
As Table 5 shows, an area that is not used for display can be used as a general data RAM.

Table 3 Correspondence between Character Codes and Character Pattern
(Hitachi Standard HD44780A00)

* The user can specify any pattern for character-generator ROM.

Table 4 Relation between CG RAM Addresses and Character Codes (DD RAM) and Character Patterns (CG RAM Data)

(a) For 5 × 7 dot character patterns



(Note) 1: Character code bits 0 ~ 2 correspond to CG RAM address bits 3 ~ 5 (3 bits: 8 types).

2: CG RAM address bits 0 ~ 2 designate character pattern line position. The 8th line is the cursor position and display is performed in logical OR by the cursor.

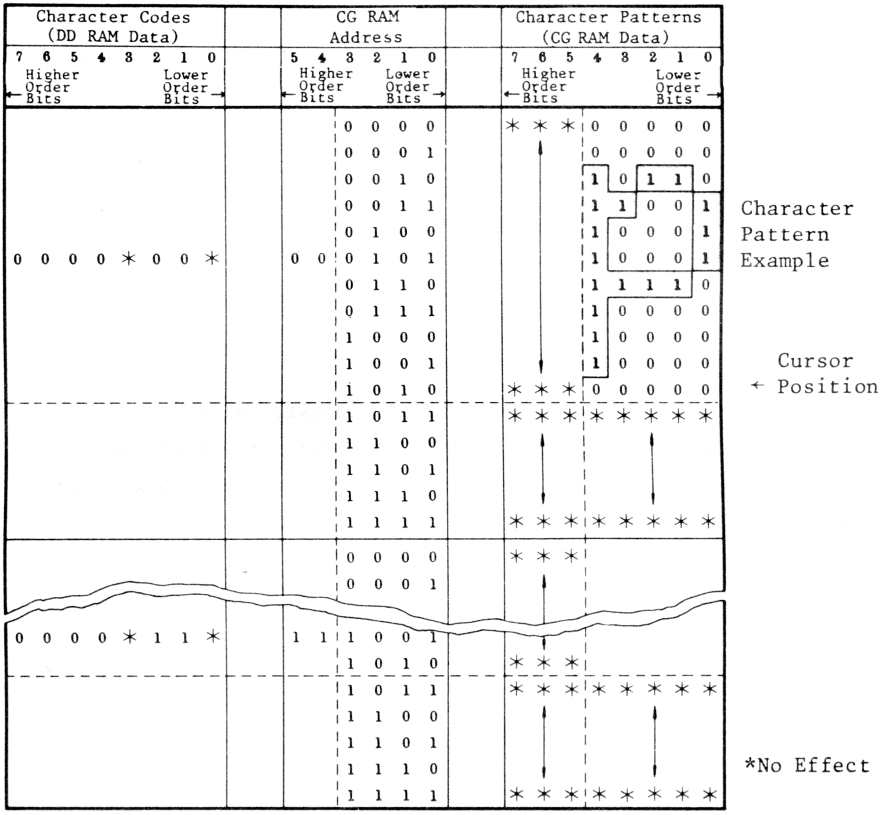
Maintain the 8th line data, corresponding to the cursor display position, in the "0" state for cursor display. When the 8th line data is "1", bit 1 lights up regardless of cursor existence.

3: Character pattern row positions correspond to CG RAM data bits 0 ~ 4, as shown in the figure (bit 4 being at the left end). Since CG RAM data bits 5 ~ 7 are not used for display, they can be used for the general data RAM.

4: As shown in Table 3 and 4, CG RAM character patterns are selected when character code bits 4 ~ 7 are all "0". However, since character code bit 3 is a ineffective bit,the "R" display in the character pattern example, is selected by character code "00" (hexadecimal) or "08" (hexadecimal).

5: "1" for CG RAM data corresponds to selection for display and "0" for non-selection.

(b) For 5 ×10 dot character patterns



(Note) 1: Character code bits 1, 2 correspond to CG RAM address bits 4, 5 (2 bits: 4 types).

2: CG RAM address bits 0 ~ 3 designate character pattern line position. The 11th line is the cursor position and display is performed in logical OR with cursor.

Maintain the 11th line data corresponding to the cursor display position in the "0" state for cursor display. When the 11th line data is "1", bit 1 lights up regardless of cursor existence. Since the 12th ~ 16th lines are not used for display, they can be used for the general data RAM.

3: Character pattern row positions are the same as 5 × 7 dot character pattern positions.

4: CG RAM character patterns are selected when character code bits 4 7 are all "0". However, since character code bit 0 and 3 are ineffective bits, "P" display in the character pattern example is selected by character code "00", "01", "08" and "09" (hexadecimal).

5: "1" for CG RAM data corresponds to selection for display and "0" for non-selection.

(7) Timing Generation Circuit

The timing generation circuit generates timing signals to operate internal circuits such as DD RAM, CG ROM and CG RAM. RAM read timing needed for display and internal operation timing by MPU access are separately generated so they do not interfere with each other. Therefore, when writing data to the DD RAM, for example, there will be no undersirable influence, such as flickering, in areas other than the display area. This circuit also generates timing signals to operate the externally connected driver LSI HD44100H.

(8) Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, the other common signal drivers continue to output non-selection waveforms.

The segment signal driver has essentially the same configuration as the driver LSI HD44100H. Character pattern data is sent serially through a 40-bit shift register and latched when all needed data has arrived. The latched data controls the driver for generating drive waveform outputs.

The serial data is sent to the HD44100H, externally connected in cascade, used for display digit number extension.

Send of serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM). Since serial data is latched when the display data character pattern, corresponding to the starting address, enters the internal shift register, the HD44780 drives the head display. The rest displays, corresponding to latter addresses, are added with each additional HD44100H.

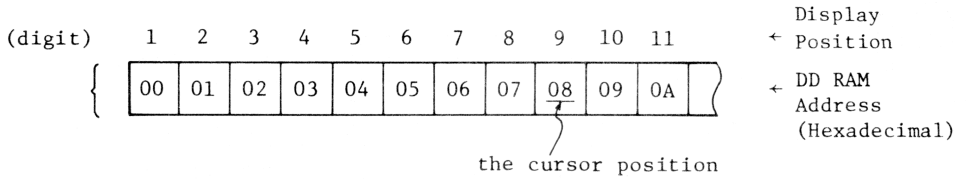
(9) Cursor/Blink Control Circuit

This is the circuit that generates the cursor or blink. The cursor or the blink appear in the digit residing at the display data RAM (DD RAM) address set in the address counter (AC).

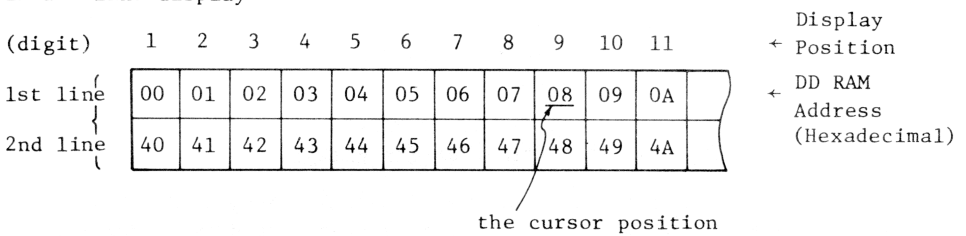
When the address counter is $(08)_{16}$, a cursor position is:

	AC6	AC5	AC4	AC3	AC2	AC1	AC0
AC	0	0	0	1	0	0	0

In a 1-line display



In a 2-line display



(Note) The cursor or blink appears when the address counter (AC) selects the character generator RAM (CG RAM). But the cursor and blink are meaningless.

The cursor or blink is displayed in the meaningless position when AC is the CG RAM address.

■ INTERFACING TO MPU

In the HD44780, data can be sent in either 4-bit 2-operation or 8-bit 1-operation so it can interace to both 4 and 8 bit MPU's.

(1) When interface data is 4-bits long, data is transferred using only 4 buses: $DB_4 \sim DB_7$. $DB_0 \sim DB_3$ are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of $DB_4 \sim DB_7$ when interface data is 8 bits long) is transferred first, then the lower order 4 bits (content of $DB_0 \sim DB_3$ when interface data is 8 bits long) is transferred.

Check the busy flag after 4-bit data has been transferred twice (one instruction). A 4-bit 2-operation will then transfer the busy flag and address counter data.

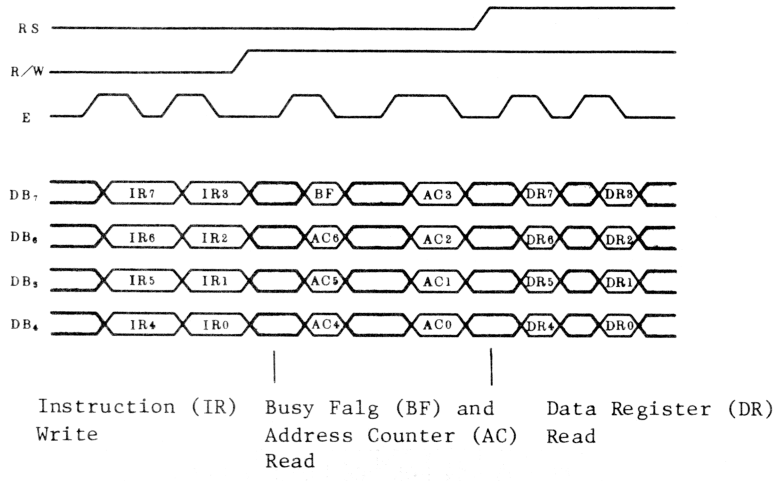


Fig. 4 4-bit Data Transfer Example

(2) When interface data is 8 bits long, data is transferred using the 8 data buses of $DB_0 \sim DB_7$.

RESET FUNCTION

● Initializing by Internal Reset Circuit

The HD44780 automatically initializes (resets) when power is turned on using the internal reset circuit. The following instructions are executed in initialization. The busy flag (BF) is kept in busy state until initialization ends. (BF=1) The busy state is 10 ms after V_{CC} rises to 4.5V.

(1) Display clear

(2) Function ser ..... DL=1 : 8 bit long interface data
N =0 : 1-line display
F =0 : 5 × 7 dot character font

(3) Display ON/OFF control ..... D =0 : Display OFF
C =0 : Cursor OFF
B =0 : Blink OFF

(4) Entry mode set ..... I/D=1: +1 (increment)
S =0 : No shift

(Note) When conditions in "Power Supply Conditions Using Internal Reset Circuit" are not met, the internal reset circuit with not operate normally and initialization will not be performed. In this case initialize by MPU according to "Initializing by Instruction".

■ INSTRUCTION

● Outline

Only two HD44780 registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the MPU. Prior to internal operation start, control information is temporarily stored in these registers, to allow interface from HD44780 internal operation to various types of MPUs which operate in different speeds or to allow interface to peripheral control ICs. HD44780 internal operation is determined by signals sent from the MPU. These signals include register selection signals (RS), read/write signals (R/W) and data bus signals ($DB_0 \sim DB_7$), and are called instructions, here. Table 5 shows the instructions and their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that,

(1) Designate HD44780 functions such as display format, data length, etc.

(2) Give internal RAM addresses.

(3) Perform data transfer with internal RAM

(4) Others

In normal use, category (3) instructions are used most frequently. However, automatic incrementing by +1 (or decrementing by -1) of HD44780 internal RAM addresses after each data write lessens the MPU program load. The display shift is especially able to perform concurrently with display data write, enabling the user to develop systems in minimum time with maximum programing efficiency. For an explanation of the shift function in its relation to display, see Table 7.

When an instruction is executing during internal operation, no instruction other than the busy flag/address read instruction will be executed. Because the busy flag is set to "1" while an instruction is being executed, check to make sure it is on "1" before sending an instruction from the MPU.

(Note) Make sure the HD44780 is not in the busy state (BF=0) before sending the instruction from the MPU to the HD44780. If the instruction is sent without checking the busy flag, the time between first and next instructions is much longer than the instruction time. See Table 5 for a list of each instruction execution time.

Table 5 Instructions

Instruction	Code										Description	Execution time (max) (when fcp or fosc is 250kHz)
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	1.64ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in adress counter. Also returns display being shifted to original position. DD RAM contents remain unchanged.	1.64ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read.	40μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of entire display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents.	40μs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (L) and character font (F).	40μs
Set CG RAM Address	0	0	0	1	ACG						Sets CG RAM address. CG RAM data is sent and received after this setting.	40μs
Set DD RAM Address	0	0	1	ADD							Sets DD RAM address. DD RAM data is sent and received after this setting.	40μs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0μs
Write Data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40μs
Read Data from CG or DD RAM	1	0	Read Data								Reads data from DD RAM or CG RAM.	40μs
	I/D=1 : Increment I/D=0 : Decrement S =1 : Accompanies display shift. S/C=1 : Display shift S/C=0 : Cursor move R/L=1 : Shift to the right. R/L=0 : Shifts to the left. DL =1 : 8 bits, DL=0 : 4 bits. N =1 : 2 lines, N=0 : 1 line F =1 : 5×10 dots, F=0 : 5×7 dots BF =1 : Internally operating BF =0 : Can accept instruction										DD RAM : Display data RAM CG RAM : Character generator RAM A_{CC} : CG RAM address A_{DD} : DD RAM address. Corresponds to cursor address. AC : Address counter used for both DD and CG RAM address.	Execution time changes when frequency changes. (Example) When fcp or fosc is 270kHz: $40\mu s \times \frac{250}{270} = 37\mu s$

* No Effect

Description of Details

(1) Clear Display

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	0	1

Writes space code "20" (hexadecimal)(character pattern for character code "20" must be blank pattern) into all DD RAM addresses. Sets DD RAM address 0 in address counter. Returns display to its original status if it was shifted. In other words, the display disappears and the cursor or blink go to the left edge of the dispaly (the first line if 2 lines are displayed). Set I/D = 1 (Increment Mode) of Entry Mode. S of Entry Mode doesn't change.

(2) Return Home

	RS	R/W	DB_7						DB_0	
Code	0	0	0	0	0	0	0	0	0	*

* Don't care

Sets the DD RAM address 0 in address counter. Returns display to its original status if it was shifted. DD RAM contents do not change. The cursor or blink go to the left edge of the display (the first line if 2 lines are displayed).

(3) Entry Mode Set

	RS	R/W	DB_7						DB_0	
Code	0	0	0	0	0	0	0	0	I/D	S

I/D: Increments (I/D=1) or decrements (I/D=0) the DD RAM address by 1 when a character code is written into or read from the DD RAM. The cursor or blink moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S : Shifts the entire display either to the right or to the left when S is 1; to the left when I/D=1 and to the right when I/D=0. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM when writing into or reading out from the CG RAM does it shift when S=0.

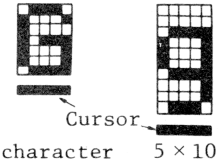
(4) Display ON/OFF Control

	RS	R/W	DB_7					DB_6
Code	0	0	0	0	0	0	1	D	C	B

D : The display is ON when D=1 and OFF when D=0. When off due to D=0, display data remains in the DD RAM. It can be displayed immediately by setting D=1.

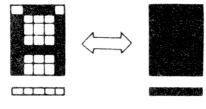
C : The cursor displays when C=1 and does not display when C=0. Even if the cursor disappears, the function of I/D, etc. does not change during display data write. The cursor is displayed using 5 dots in the 8th line when the 5 × 7 dot character font is selected and 5 dots in the 11th line when the 5 × 10 dot character font is selected.

B : The character indicated by the cursor blinks when B=1. The blink is displayed by switching between all blank dots and display characters at 409.6ms interval when fcp or fosc=250kHz. The cursor and the blink can be set to display simultaneously. (The blink frequency changes according to the reciprocal of fcp or fosc. $409.6 \times \frac{250}{270} = 379.2$ms when fcp=270kHz.)



5 × 7 dot character font　　5 × 10 dot character font

(a) Cursor Display Example



Alternating display

(b) Blink Display Example

(5) Cursor or Display Shift

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* Don't care

Shifts cursor position or display to the right or left without writing or reading display data. This function is used to correct or search for the display. In a 2-line display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time. When the displayed data is shifted repeatedly each line only moves horizontally. The 2nd line display does not shift into the 1st line postion.

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Address counter (AC) contents do not change if the only action performed is shift display.

(6) Function Set

	RS	R/W	DB7						DB0
Code	0	0	0	0	1	DL	N	F	*	*

* (Don't care)

DL : Sets interface data length. Data is sent or received in 8 bit lengths ($DB_7 \sim DB_0$) when DL=1 and in 4 bit lengths ($DB_7 \sim DB_4$) when DL=0.

When the 4 bit length is selected, data must be sent or received twice.

N : Sets number of display lines.

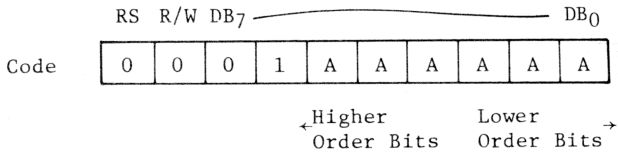
F : Sets character font.

(Note) Perform the function at the head of the program before executing all instructions (except "Busy flag/address read"). From this point, the function set instruction cannot be executed unless the interface data length is changed.

N	F	No. of display lines	Character font	Duty factor	Remarks
0	0	1	5 ×7 dots	1/8	
0	1	1	5 ×10 dots	1/11	
1	*	2	5 ×7 dots	1/16	Cannot display 2 lines with 5 ×10 dot character font.

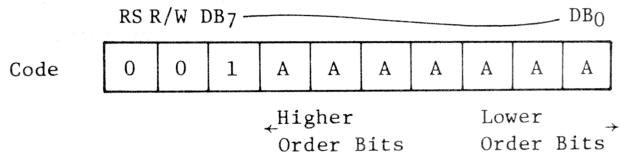
* (Don't care)

(7) Set CG RAM Address



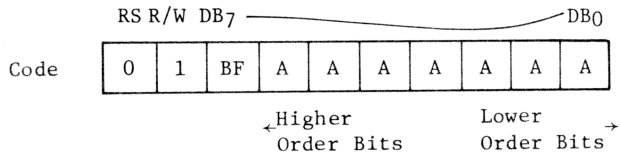
Sets the CG RAM address into the address counter in binary AAAAAA. Data is then written or read from the MPU for the CG RAM.

(8) Set DD RAM Address



Sets the DD RAM address into the address counter in binary AAAAAAA. Data is then written or read from the MPU for the DD RAM.
However, when N=0 (1-line display), AAAAAAA is "00" ~ "4F" (hexadecimal).
when N=1 (2-line display), AAAAAAA is "00" ~ "27" (hexadecimal) for the first line, and "40" ~ "67" (hexadecimal) for the second line.

(9) Read Busy Flag and Address



Reads the busy flag (BF) that indicates the system is now internally operating by a previously received instruction. BF=1 indicates that internal operation is in progress. The next instruction will not be accepted until BF is set to "0". Check the BF status before the next wire operation.

At the same time, the value of the address counter expressed in binary AAAAAAA is read out. The address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. Address contents are the same as in Items (7) and (8).

(10) Write Data to CG or DD RAM

	RS	R/W	DH_7							DB_0
Code	1	0	D	D	D	D	D	D	D	D

← Higher Order Bits Lower Order Bits →

Writes binary 8 bit data DDDDDDDD to the CG or the DD RAM.

Whether the CG or DD RAM is to be written into is determined by the previous specification of CG RAM or DD RAM address setting. After write, the address is automatically incremented or decremented by 1 according to entry mode. The entry mode also determines display shift.

(11) Read Data from CG or DD RAM

	RS	R/W	DB_7							DB_0
Code	1	1	D	D	D	D	D	D	D	D

← Higher Order Bits Lower Order Bits →

Reads binary 8 bit data DDDDDDDD from the CG or DD RAM.

The previous designation determines whether the CG or DD RAM is to be read. Before entering the read instruction, you must execute either the CG RAM or DD RAM address set instruction. If you don't, the first read data will be invalidated. When serially executing the "read" instruction, the next address data is normally read from the second read. The "address set" instruction need not be executed just before the "read" instruction when shifting the cursor by cursor shift instruction (when reading out DD RAM). The cursor shift in struction operation is the same as that of the DD RAM's address set instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed no matter what the entry mode is.

(Note) The address counter (AC) is automatically incremented or decremented by 1 after "write" instructions to either CG RAM or DD RAM. RAM data selected by the AC cannot then be read out even if "read" instructions are executed. The conditions for correct data read out are: execute either the address set

instruction or cursor shift instruction (only with DD RAM), just before reading out execute the "read" instruction from the second time the "read" instruction is serial.

■ HOW TO USE THE HD44780

● Interface to MPU

(1) Interface to 8-bit MPU

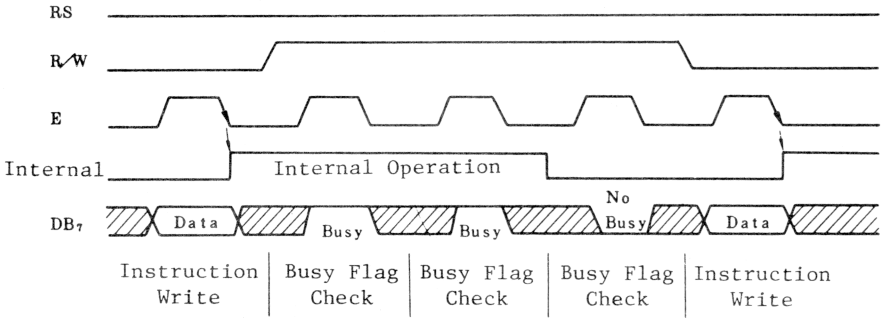
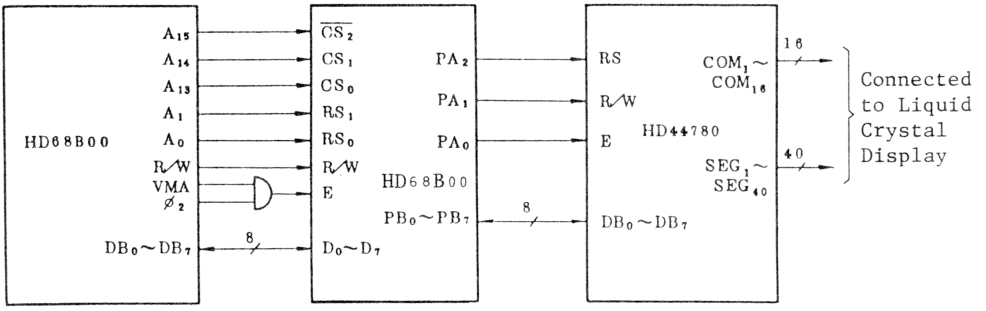


Fig. 5 Example of Busy Flag Check Timing Sequence

① When connecting to 8-bit MPU through PIA

Fig. 6-2 is an example of using a PIA or I/O port (for single chip microcomputer) as an interface device. Input and output of the device is TTL compatible.

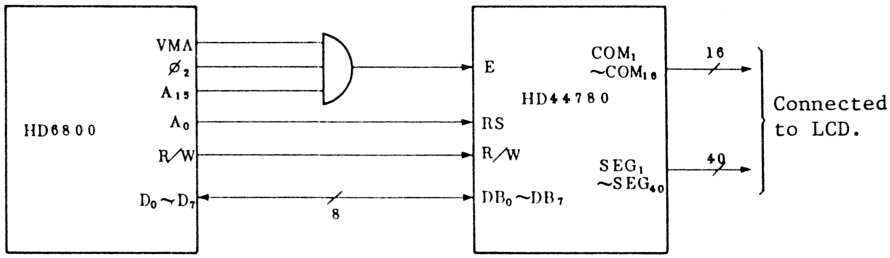
In the example, PB_0 to PB7 are connected to the data buses DB_0 to DB7 and PA0 to PA2 are connected to E, R/W and RS respectively. Pay attention to the timing relation between E and other signals when reading or writing data and using PIA as an interface.



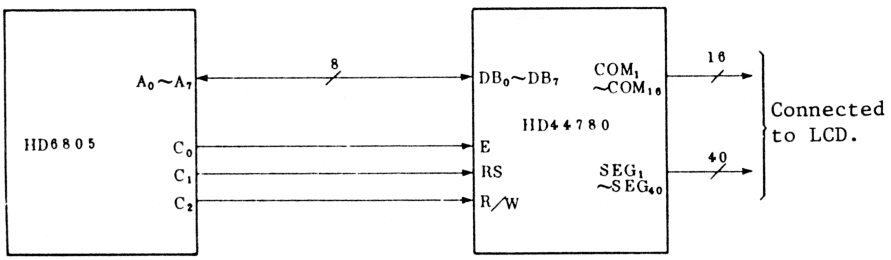
HD68B00: 8 bit CPU

Fig. 6 Example of Interface to HD68B00 Using PIA (HD68B21)

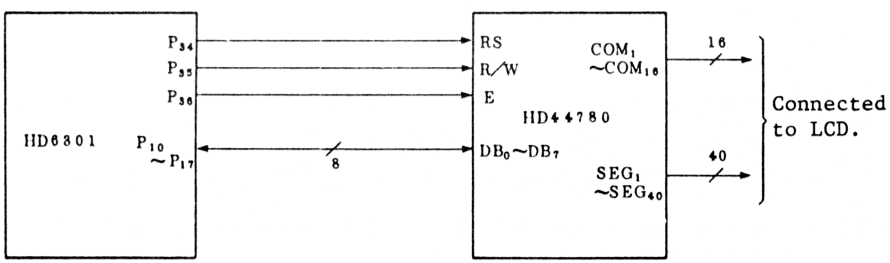
② Connecting directly to the 8-bit MPU bus line



③ Example of interfacing to the HD6805



④ Example of interfacing to the HD6301

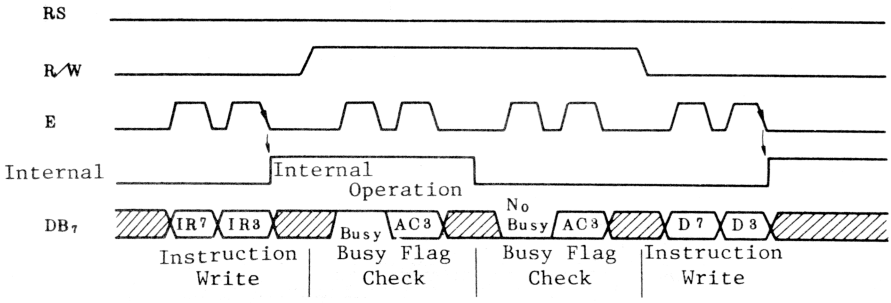


(2) Interface to 4-bit MPU

The HD44780 can be connected to a 4-bit MPU through the 4-bit MPU I/O port. If the I/O port has enough bits, data can be transferred in 8-bit lengths, but if the bits are insufficient, the transfer is made in two operations of 4 bits each (with designation of interface data length for 4 bits). In the latter case, the timing sequence becomes somewhat complex. (See Fig. 7)

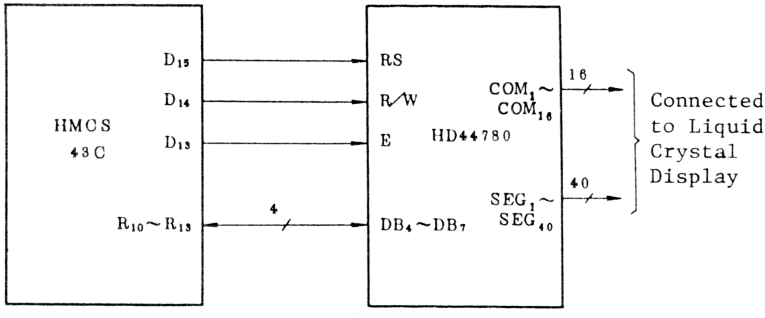
Fig. 8 shows an example of interface to the HMCS43C.

Note that 2 cycles are needed for the busy flag check as well as the data transfer. 4-bit operation is selected by program.



(Note) IR7, IR3: Instruction 7th bit, 3rd bit
AC3 : Address Counter 3rd bit

Fig. 7 An Example of 4-bit Data Transfer Timing Sequence



HMCS43C: Hitachi 4-bit single-chip microcomputer

Fig. 8 Example of Interface to the HMCS43C

Interface to Liquid Crystal Display

(1) Character Font and Number of Lines

The HD44780 can perform 2 types of display, 5 ×7 dots and 5 ×10 dots as character font, with a cursor on each.

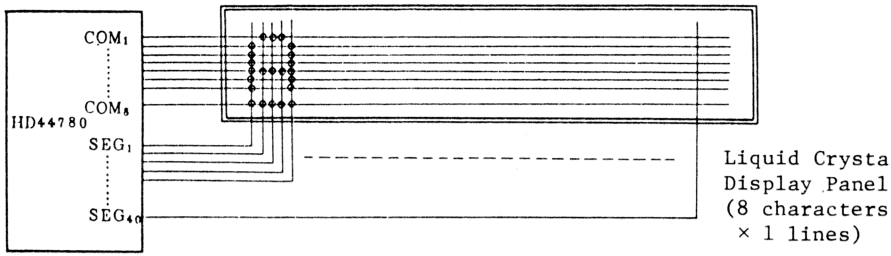
Up to 2 lines are displayed with 5 ×7 dots and 1 line with 5 ×10 dots. Therefore, three types of common signals are available:

Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	5 ×7 dots + Cursor	8	1/8
1	5 ×10 dots + Cursor	11	1/11
2	5 ×7 dots + Cursor	16	1/16

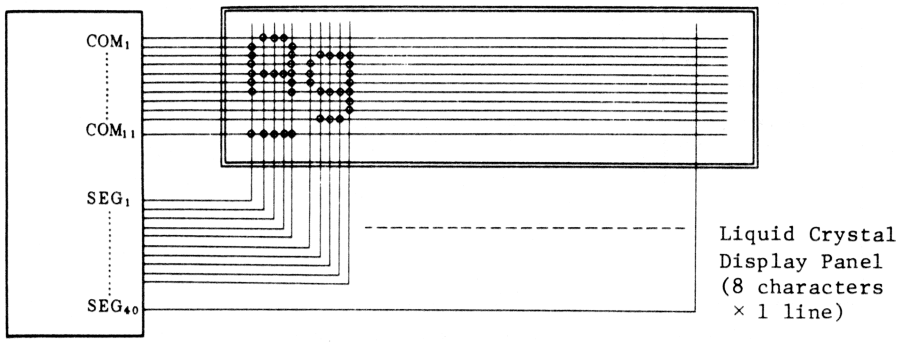
Number of lines and font types can be selected by program.
(See to Table 5 Instruction)

(2) Connection to HD44780 and Liquid Crystal Display

Fig. 9 (1) and (2) show connection examples.

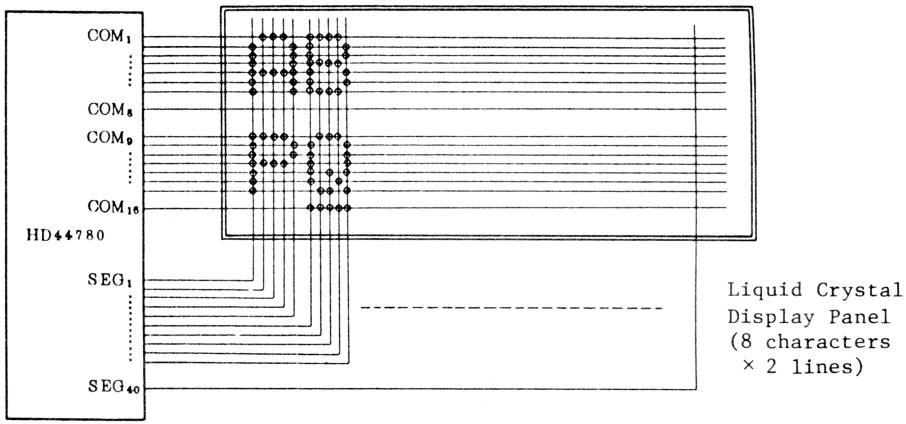


(a) Example of a 5 ×7 dot, 8 character × 1 line Display (1/4 Bias, 1/8 Duty)



(b) Example of a 5 ×10 dot, 8 character × 1 line Display (1/4 Bias, 1/8 Duty)

Fig. 9 (1) Liquid Crystal Display and Connections to HD44780

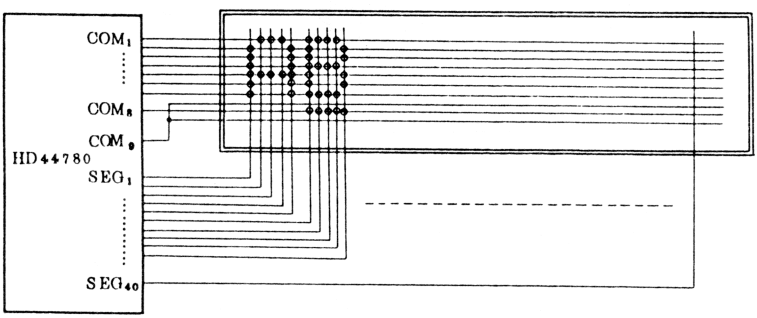


(c) Example of 5 × 7 dot, 8 character × 2 lines Display (1/5 Bias, 1/16 Duty)

Fig. 9 (2) Liquid Crystal Display and Connection to HD44780

Since 5 signal lines at the SEG can display one digit, one HD44780 can display up to 8 digits for 1-line display and 16 digits for 2-line display.

In Fig. 9 examples (a) and (b), there are unused common signal terminals, non-selection waveforms which always output. When the liquid crystal display panel has unused extra scanning lines, avoid undesirable influences due to cross-talk in the floating state by connecting the extra scanning lines to these common signal terminals.

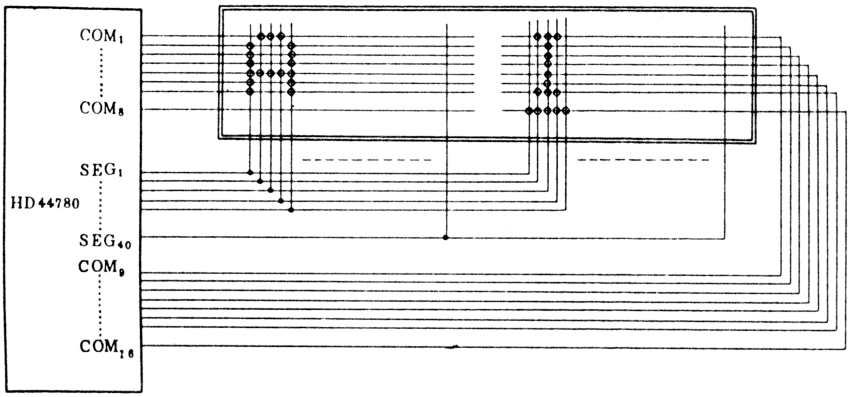


5 × 7 dot, 8 character × 1 line Display (1/4 Bias, 1/8 Duty)

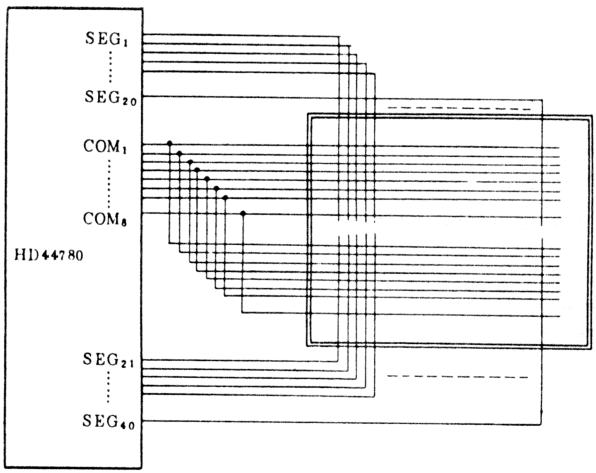
Fig. 10 Using COM9 to Avoid Cross-talk on Unneeded Scanning Line

(3) Connection of Changed Matrix Layout

In the preceding examples, the number of lines was matched to the number of scanning lines. The following display types are possible by changing the matrix layout in the liquid crystal display panel.



(a) 5 × 7 dot, 16 character × 1 line Display
(1/5 Bias, 1/16 Duty)



(b) 5 × 7 dot, 4 character × 2 line Display
(1/4 Bias, 1/8 Duty)

Fig. 11 Changed Matrix Layout Displays

In either case, the only change is the layout. Display characteristics and the number of liquid crystal display characters are dependent on the number of common signals (or duty factor). Note that the display data RAM (DD RAM) addresses for 8 characters × 2 lines and 16 characters × 1 line are the same as shown in Fig. 9.

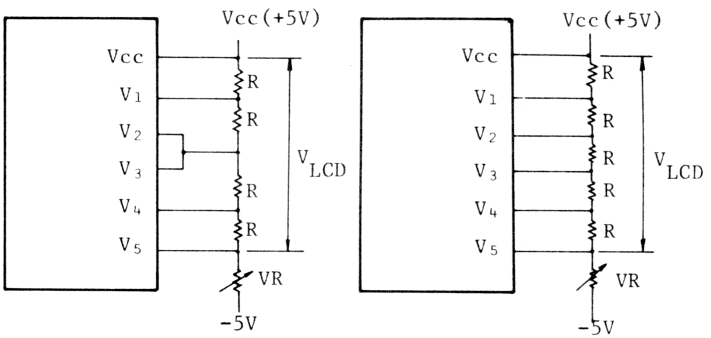
● Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to HD44780 terminals V_1 to V_5 to obtain liquid crystal display drive waveforms. The voltages must be changed according to duty factor. Table 6 shows the relation.

Table 6 Duty Factor and Power Supply for Liquid Crystal Display Drive

Duty Factor / Power Supply Bias	1/8, 1/11	1/16
	1/4	1/5
V_1	$V_{cc} - 1/4\ V_{LCD}$	$V_{cc} - 1/5\ V_{LCD}$
V_2	$V_{cc} - 1/2\ V_{LCD}$	$V_{cc} - 3/5\ V_{LCD}$
V_3	$V_{cc} - 1/2\ V_{LCD}$	$V_{cc} - 3/5\ V_{LCD}$
V_4	$V_{cc} - 3/4\ V_{LCD}$	$V_{cc} - 4/5\ V_{LCD}$
V_5	$V_{cc} - V_{LCD}$	$V_{cc} - V_{LCD}$

V_{LCD} gives the peak values for liquid crystal display drive waveforms. Resistance dividing provides each voltage as shown in Fig. 13.



(a) 1/4 Bias (1/8, 1/11 Duty)

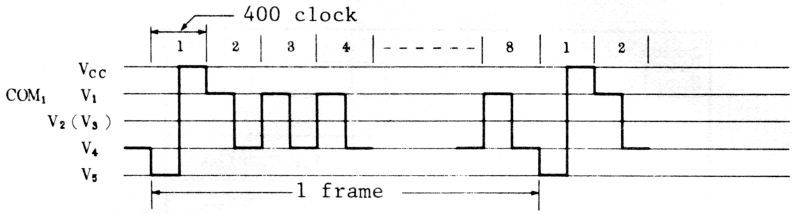
(b) 1/5 Bias (k/16 Duty)

Fig. 13 Drive Voltage Supply Example

● Relation between Oscillation Frequency and Liquid Crystal Display Frame Frequency

The following examples of liquid crystal display frame frequency apply only when oscillation frequency is 250kHz. (1 clock = 4μs)

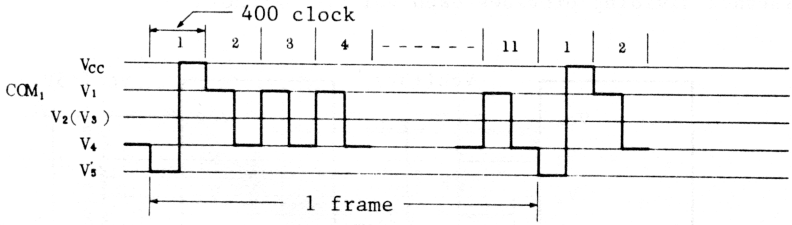
(1) 1/8 Duty



1 frame = 4 (μs) × 400 × 8 = 12800 (μs) = 12.8 (ms)

$$\text{Frame frequency} = \frac{1}{12.8\ (\text{ms})} = 78.1\ (\text{Hz})$$

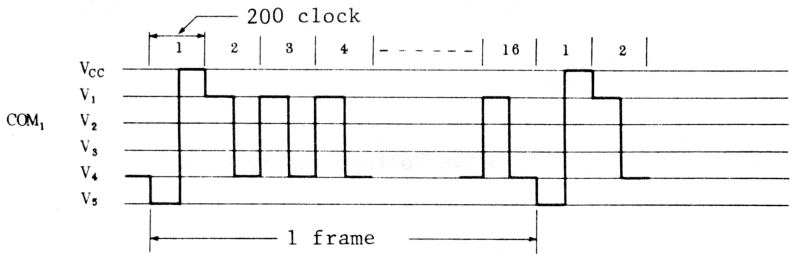
(2) 1/11 Duty



1 frame = 4 (μs) × 400 × 11 = 17600 (μs) = 17.6 (ms)

$$\text{Frame frequency} = \frac{1}{17.6\ (\text{ms})} = 56.8\ (\text{Hz})$$

(3) 1/16 Duty



1 frame = 4 (μs) × 200 × 16 = 12800 (μs) = 12.8 (ms)

$$\text{Frame frequency} = \frac{1}{12.8\ (\text{ms})} = 78.1\ (\text{Hz})$$

● Connection with Driver LSI HD44100H

You can increase the number of display digits by externally connecting a liquid crystal display driver LSI HD44100H to the HD44780.

When connected to the HD44780, the HD44100H is used as segment signal driver. The HD44100H can be connected to the HD44780 directly since it supplies CL_1, CL_2, M and D signals and power for liquid crystal display drive. Fig. 14 shows a connection example.

Caution: Connection of voltage supply terminals V_1 through V_6 for liquid crystal display drive is complicated.

Up to 9 units of the HD44100H can be connected for 1-line display (duty factor 1/8 or 1/11) and up to 4 units for the 2-line display (duty factor 1/16). RAM size limits the HD44780 to a maximum of 80 character display digits. The connection method in Fig. 14 remains unchanged for both 1-line and 2-line display or both 5 ×7 and 5 ×10 dot character fonts.

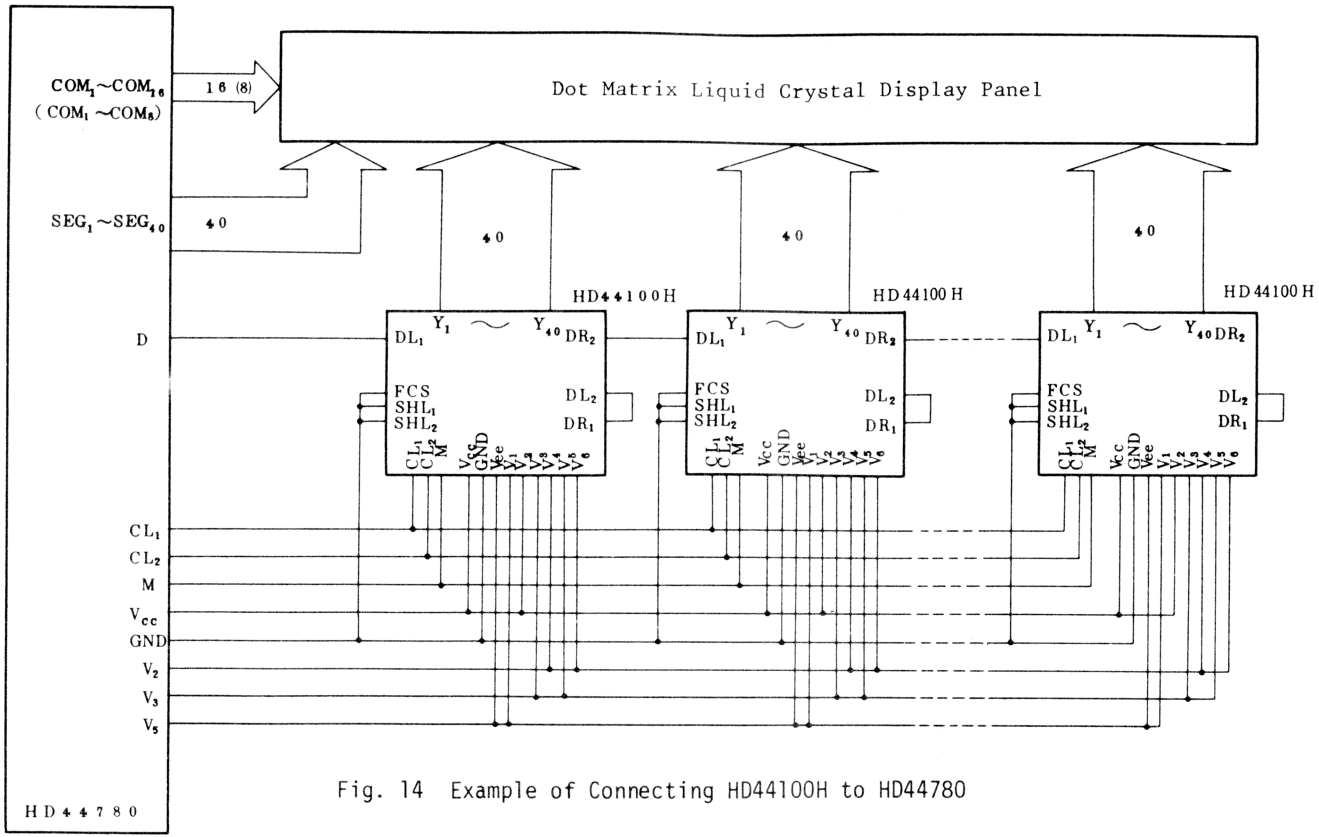


Fig. 14 Example of Connecting HD44100H to HD44780

● Instruction and Display Correspondence

(1) 8-bit operation, 8-digit × 1-line display (using internal reset)

Table 7 shows an example of 8-bit × 1-line display in 8-bit operation.

The HD44780 functions must be set by Function Set prior to display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays like the lightening board when combined with display shift operation.

Since the display shift operation changes display position only and DD RAM contents remain unchanged, display data entered first can be output when the return home operation is performed.

(2) 4-bit operation, 8-digit × 1-line display (using internal reset)

The program must set functions prior to 4-bit operation. Table 8 shows an example. When power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since nothing is connected to $DB_0 \sim DB_3$, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is needed as a function (see Table 8).

Thus, $DB_4 \sim DB_7$ of the function set is written twice.

(3) 8-bit operation, 8-digit × 2-line display

For 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the 1st line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must again be set after the 8th character is completed. (See Table 9) Note that the first and second lines of the display shift are performed. In the example, the display shift is performed when the cursor is on the second line. However, if shift operation is performed when the cursor is on the first line, both the first and second lines move together. When you repeat the shift, the display of the second line will not move to the first line, the same display will only move within each line many times.

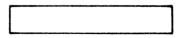
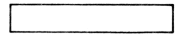
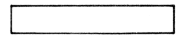
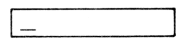
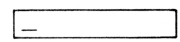
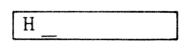
(Note) When using the internal reset, the conditions in "Power Supply Condition Using Internal Reset Circuit" must be satisfied. If not, the HD44780 must be initialized by instruction. (See "Initializing by Instruction")

Table 7 8-bit Operation, 8-digit 1-line Display Example(Using Internal Reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 ~ DB_0 0 0 0 0 1 1 0 0 * *		Sets to 8-bit operation and selects 1-line display lines and character font. (Number of display lines and character fonts cannot be changed hereafter.)
3	Display ON/OFF Control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Write "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HI_	Writes "I".
7	⋮	⋮	
8	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
9	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI_	Sets mode for display shift at the time of write.
10	Write Data to CG RAM/DD RAM 1 0 0 0 1 0 0 0 0 0	ITACHI _	Writes "Space".
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	TACHI M_	Writes "M".
12	⋮	⋮	

13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	MICROKO_	Writes "0".
14	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
15	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
16	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 0 0 1 1	ICROCO	Writes "C" (correction). The display moves to the left.
17	Cursor or Display Shift 0 0 0 0 0 1 1 1 * *	MICROCO	Shifts the display and cursor position to the right.
18	Cursor or Display Shift 0 0 0 0 0 1 0 1 * *	MICROCO_	Shifts display and cursor position to the right.
19	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ICROCOM_	Writes "M".
20	⋮	⋮	
21	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI	Returns both display and cursor to the original position (Address 0).

Table 8 4-bit Operation, 8-digit 1-line Display Example (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB7 ⌒ DB4 0 0 0 0 1 0		Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
3	Function Set 0 0 0 0 1 0 0 0 0 0 * *		Sets 4-bit operation and selects 1-line display and 5×7 dot character font. 4-bit operation starts from this point on and resetting is needed. (Number of display lines and character fonts cannot be changed hereafter.)
4	Display ON/OFF Control 0 0 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. Entire display is in space mode because of initialization.
5	Entry Mode Set 0 0 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 1 0 0 0		Writes "H". The cursor is incremented by one and shifts to the right.

Hereafter, control is the same as 8-bit operation.

Table 9 8 bit Operation, 8-digit × 2 line Display Example (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is intialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 ... DB_0 0 0 0 0 1 1 1 0 * *		Sets to 8-bit operation and selects 2-line display and 5×7 dot character font.
3	Display ON/OFF Control 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. All display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H	Writes "H". The DD RAM has has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	⋮	⋮	
7	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI	Writes "I".
8	Set DD RAM Address 0 0 1 1 0 0 0 0 0 0	HITACHI	Sets RAM address so that the cursor is positioned at the head of the 2nd line.
9	Write Data co CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	HITACHI M	Writes "M".
10	⋮	⋮	
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	HITACHI MICROCO	Writes "O".
12	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI MICROCO	Sets mode for display shift at the time of write.

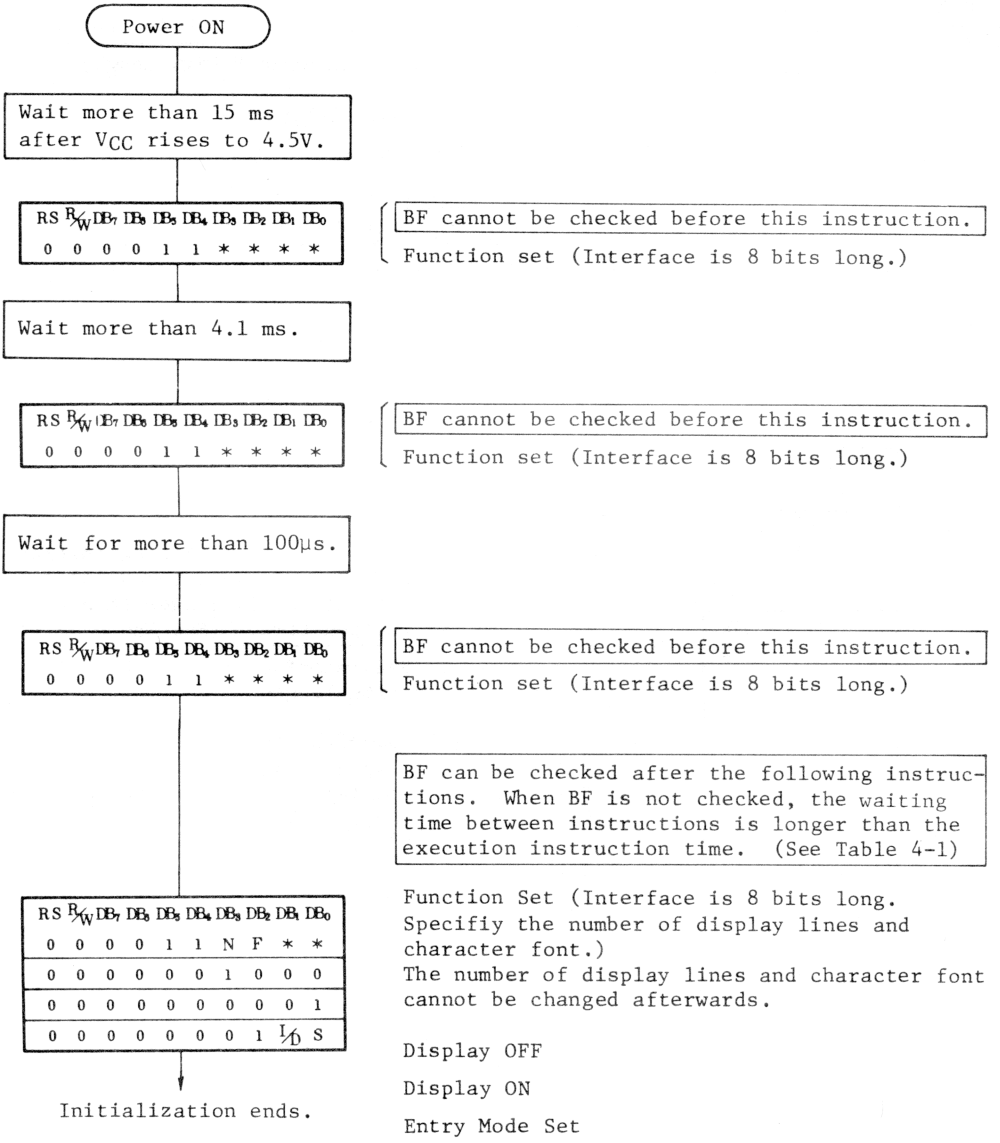
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ITACHI ICROCOM_	Writes "M". Display is shifted to the right. The first and second lines' shift are operated at the same time.
14	⋮	⋮	
15	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI MICROCOM	Returns both display and cursor to the original position (Address 0).

● Initializing by Instruction

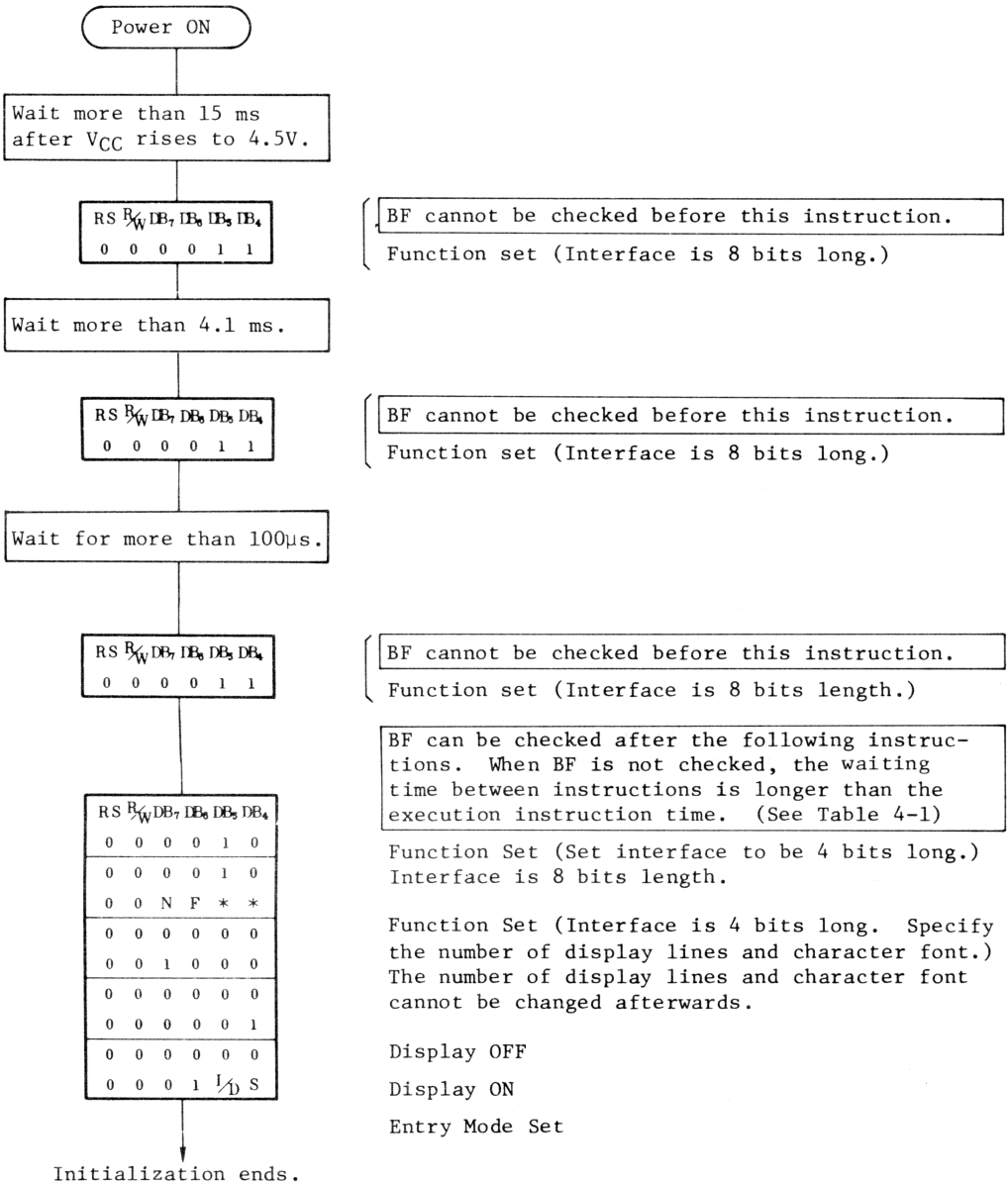
If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instruction is required.

Use the following procedure for initialization.

(1) When interface is 8 bits long;



(2) When interface is 4 bits long;



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