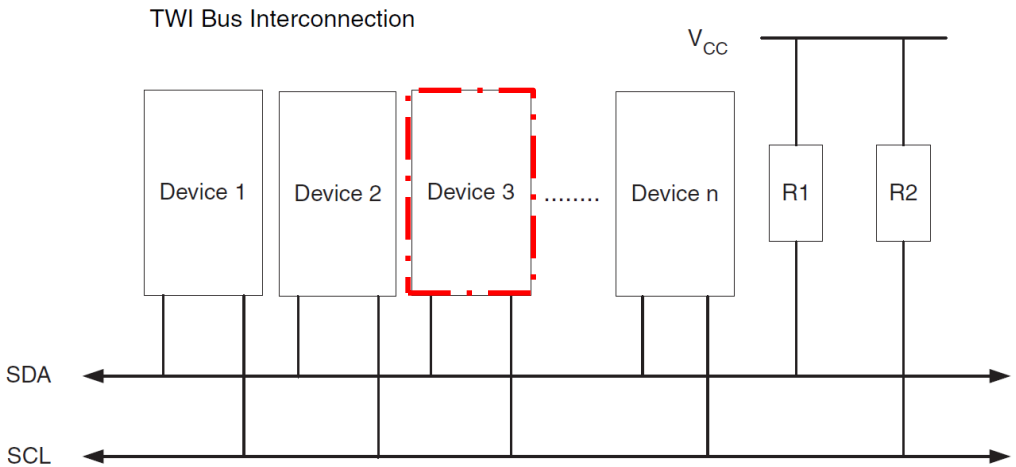
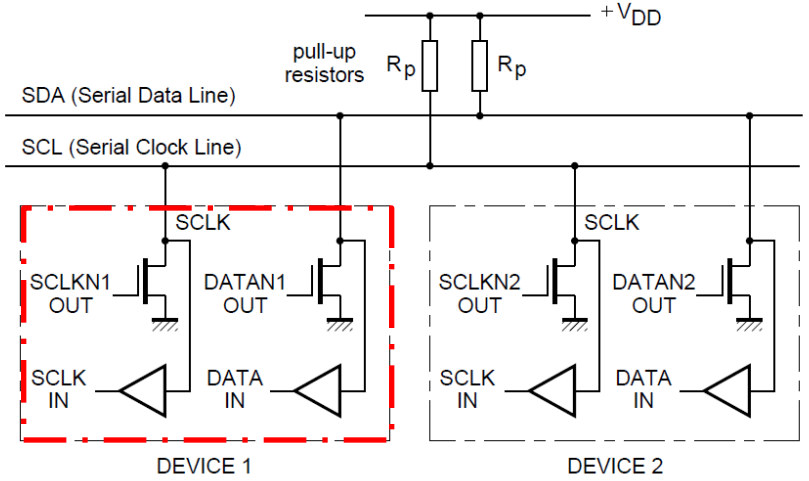
I2C (TWI) — *Inter Integrated Circuit*

- **I2C** je sériová synchronná zbernica vyvinutá firmou Philips.
- Na **I2C** zbernicu možno pripojiť EEPROM, ADC, LCD budiče, (>1000 IC's)
- Počet obvodov pripojených na zbernicu je obmedzený počtom adries a celkovou kapacitou zbernice <400 **pF** („jednotkou dĺžky je **pF**“).
- Na prenos informácie sú použité dve nesymetrické vedenia
  - SCL (hodiny)
  - SDA (data)

Tieto vodiče sú obojsmerné a pomocou PULLED UP rezistorov ťahané hore. Všetky zariadenia pripojené na zbernicu musia mať „otvorený kolektor“. Budiče zbernice majú implementované „drôtové AND“.





I2C *Inter Integrated Circuit*

- Každé zariadenie pripojené k zbernici je identifikované
  7-, resp. (128 zariadení *mínus* 16 rezervovaných = 112)
  10-bitovou adresou (1024 zariadení *mínus* rezervované adresy = 1008
  „mostíkom“ je rezervovaná adresa 1111 0XX).
- Módy prenosu (prenosová rýchlosť):
  - **Standard mode**: <100kb/s
  - **Fast mode**: <400kb/s
  - **Fast mode plus**: <1000kb/s
  - **High-speed mode:** <3400kb/s (10bit adresa, až 1024 zariadení)

I2C - (TWI)

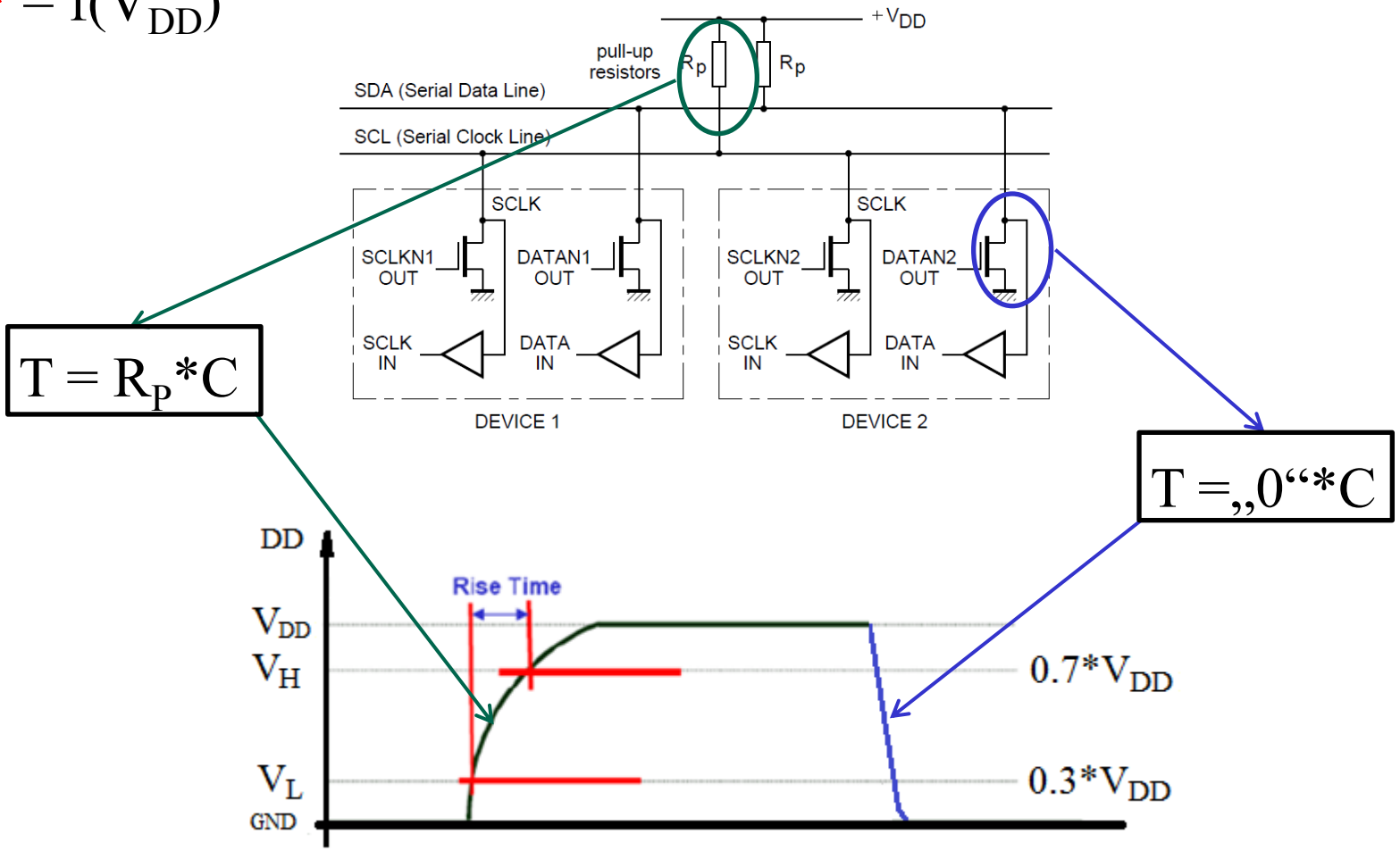
Dôležité pojmy:

- **Transmitter** – zariadenie vysielajúce dáta na zbernicu.
- **Receiver** –zariadenie prijímajúce data zo zbernice.
- **Master** – inicializujúce (zahajuje) prenos na zbernici, generuje hodinové signály a ukončuje prenos. MASTER môže byť vo funkcii vysielača aj prijímača.
- **Slave** – zariadenie adresované MASTER-om. SLAVE môže byť aj vysielač aj prijímač.
- **Multi-master** – schopnosť súčasnej koexistencie viacerých MASTER-ov na zbernici bez kolízií a strát dát.
- **Arbitration** – vlastnosť, ktorá zabezpečí, že v danom čase len jeden MASTER riadi zbernicu.
- **Synchronization** – vlastnosť, ktorá zabezpečí, synchronizáciu hodinových signálov, ktoré generujú dve, resp. viaceré zariadenia typu MASTER.

I2C

Zdroj:
Log. 1
Log. 0
= f(V_{DD})

Prijímač filtruje krátke impulzy na zbernici.



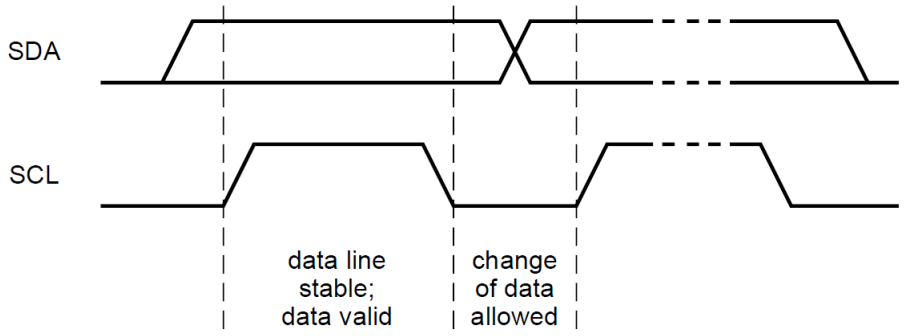
I2C protokol:
Prenos dát a formáty prenášaného rámca

- Data sú po SDA prenášané bytovo. Niekoľko bytov ohraničených **S** a **P**.
- Na prenesenie jedného Byte je generovaný MASTER-om
  - 8-f_{I2C} pre data a
  - 1-f_{I2C} pre ACK. Prijímač potvrdzuje ACK.

    Tento jeden bit „vysiela“ prijímač.

- **Prenos bitu(ov)**

  Prenos bitu je podmienený jedným pulzom na SCL. Signál na SDA vodiči musí byť stabilný ak je CLK signál v úrovni Log. 1.



Bit transfer on the I²C-bus.

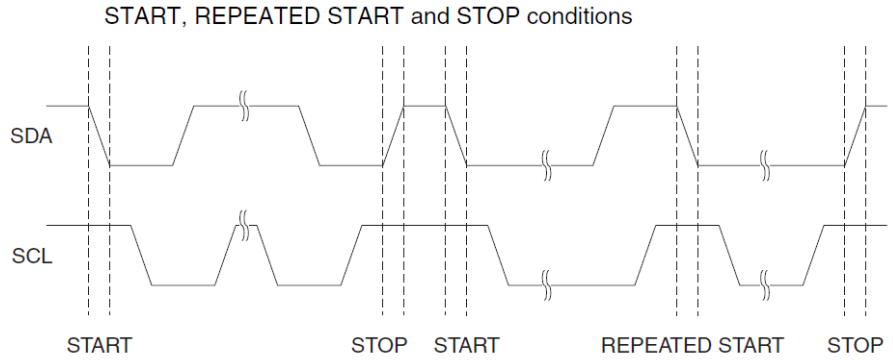
Jediná výnimka z tohto pravidla je mechanizmus generovania

Start a sto**P** podmienky.

I2C protokol:

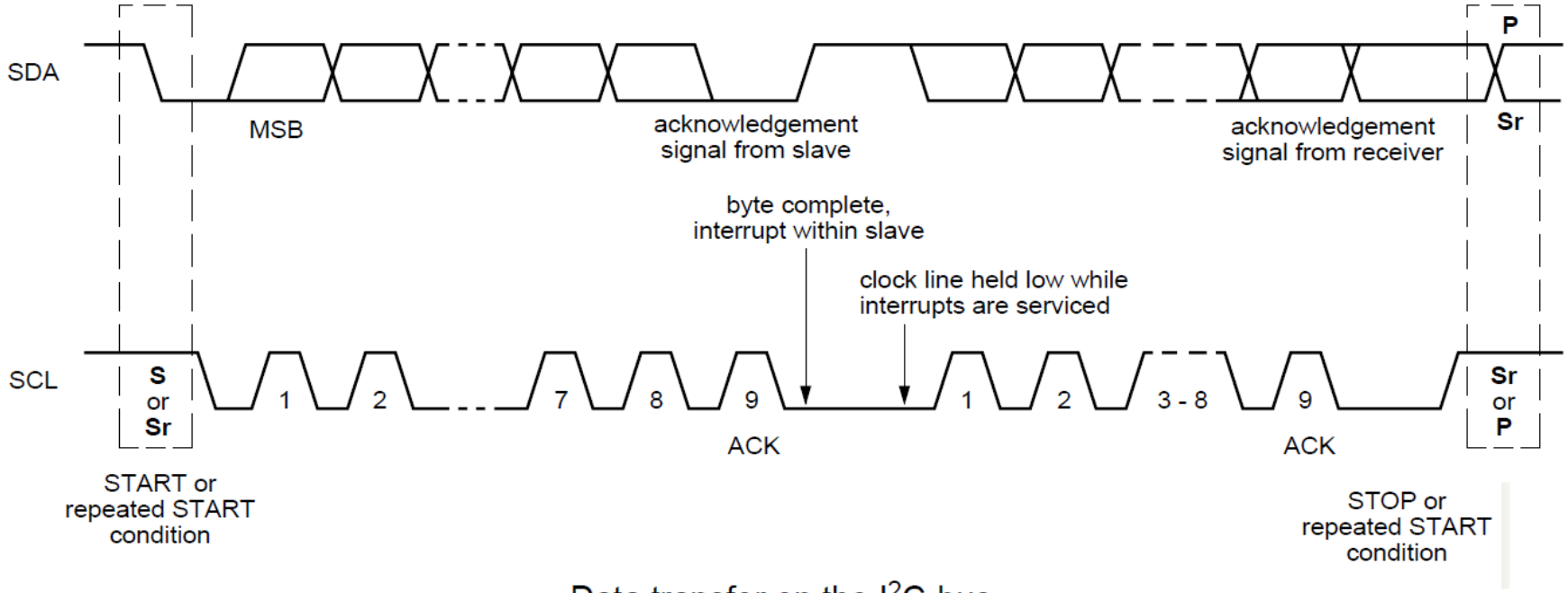
Prenos Start a stoP podmienky.

- Ak je zbernica voľná, môže sa uskutočniť prenos. T.j. oba vodiče sú v logickej jednotke.
- MASTER inicializuje a ukončuje prenos.
  - Prenos sa začne, ak MASTER odvysiela **S**tart podmienku
  - prenos sa ukončí, ak MASTER odvysiela sto**P** podmienku.
  - Zbernica je medzi **S**tart a sto**P** podmienkou v stave „busy“.
  - Ak sa medzi **S**tart a sto**P** podmienkou objaví opakovaný **S**tart, tento stav sa označuje ako REPEATED **S**tart podmienka (Sr, S).
  - **S**tart a sto**P** podmienka sa realizujú ako zmena na SDA počas vysokej úrovne na SCL vodiči.



I2C protokol:

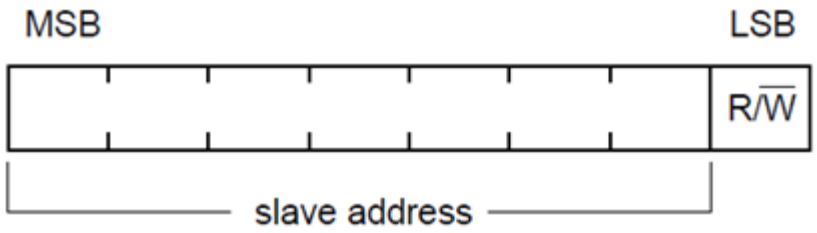
- Všetky vysielané data pomocou I2C zbernice sú 9 bitové.



Data transfer on the I²C-bus.

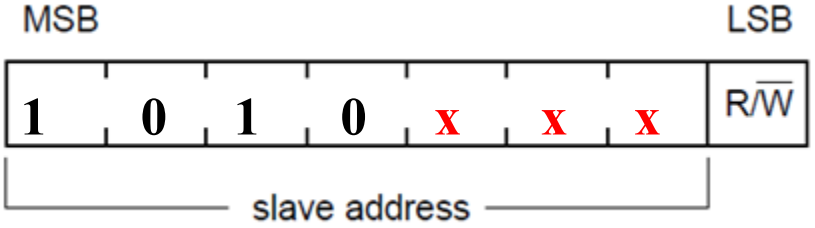
I2C protokol:

- Prvý byte (niekedy sa nazýva riadiaci byte) po **Start** podmienke je rozdelený na:
- 7 bitov - adresa – (Pevná a programovateľná časť)
- 1 bit - Read/Write riadiaci bit . Tento bit nastavuje typ operácie.
- 1 bit – acknowledge bit (ACK). Ak adresované zariadenie rozpozná svoju adresu, potvrdí to tak, že počas 9-teho SCL hodinového signálu stiahne SDA na nízku úroveň. MASTER potom môže odvysielať sto**P** podmienku alebo opakovaný **Start**, aby mohol inicializovať nový prenos. Adresný packet pozostávajúci z adresy SLAVE zariadenia a READ alebo WRITE podmienky sa označuje: SLA+R resp. SLA+W.



I2C protokol: „riadiaci byte“

- 7 bitov - adresa – (Pevná a programovateľná časť)



- 10bitová adresa

Table 2 Definition of bits in the first byte

SLAVE ADDRESS	R/W BIT	DESCRIPTION
0000 000	0	General call address
0000 000	1	START byte(1)
0000 001	X	CBUS address(2)
0000 010	X	Reserved for different bus format(3)
0000 011	X	Reserved for future purposes
0000 1XX	X	Hs-mode master code
1111 1XX	X	Reserved for future purposes
1111 0XX	X	10-bit slave addressing

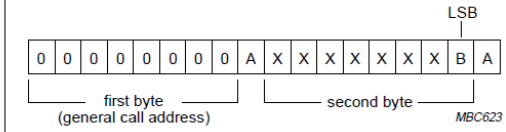
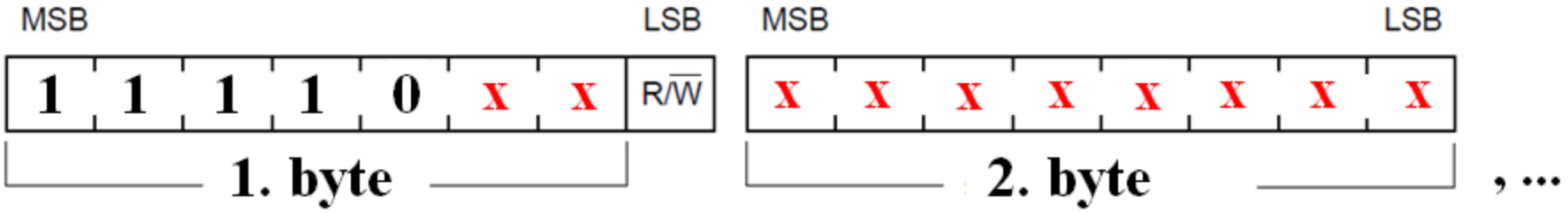


Fig.15 General call address format.

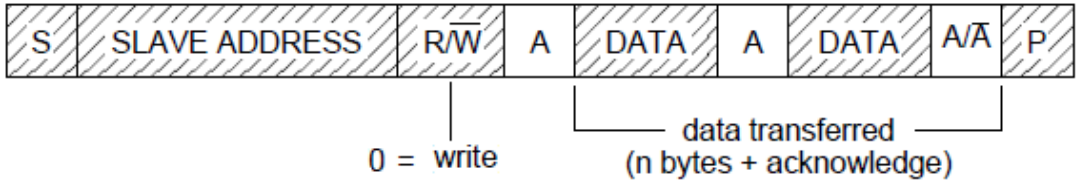
When bit B is a ‘zero’; the second byte has the following definition:

- 00000110 (H‘06’). Reset and write programmable part of slave address by hardware.



I2C protokol:

MASTER (TRANSMITTER) – SLAVE (RECEIVER)



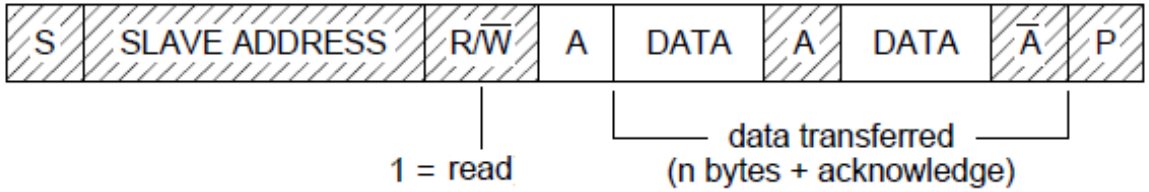
A master-transmitter addressing a slave receiver with a 7-bit address.
The transfer direction is not changed.

from master to slave

from slave to master

A = acknowledge (SDA LOW)
Ā = not acknowledge (SDA HIGH)
S = START condition
P = STOP condition

MASTER (RECEIVER) – SLAVE (TRANSMITTER)



A master reads a slave immediately after the first byte.

I2C protokol:
Riešenie problémov na zbernici

Riešenie konfliktov je založené na počúvaní.

Vysielač „budí znernicu“ a zároveň kontroluje, či sa na zbernici objaví to, čo vysielač na zbernicu poslal:

- Log.1 – mäkký zdroj signálu
- Log. 0 – tvrdý zdroj signálu

  Dva dôvody, že sa neobjaví Log. 1

  – Log. 1 (*) Log. 0 = Log. 0.

  Dôvod tohto stavu. Napr.: Iný Master (Log. 0) pôsobiaci na zbernici

  – Mäkký zdroj Log. 1.

  Dôvod tohto stavu. Vysielač nedokáže v danom čase „nabiť“ cele vedenie (celú kapacitu)

Synchronný prenos:
môžeme spomaliť, pozastaviť

Pomalšie zariadenie (SLAVE) môže

– **spomaliť**. SLAVE zariadenie môže v každej perióde podržať SCL na log. 0.

– **pozastaviť**. Ak potrebuje SLAVE zariadenie čas na spracovanie dát podrží SCL na úrovni log. 0 po ACK bite.

MultiMaster režim:

MASTER – inicializujúce (zahajuje) prenos na zbernici, generuje hodinové signály a ukončuje prenos. MASTER môže byť vo funkcii vysielača aj prijímača. Ak je na zbernicu pripojený len jeden MASTER, je komunikácia po zbernici jednoduchá. Ak je na zbernicu pripojených viacero MASTER-ov, treba určiť, kto v danom stave riadi zbernicu. Treba riešiť dve úlohy:

– **synchronizáciu hodín** (SCL)**:** Ak čo i len jeden MASTER nastaví SCL na Log. 0, zbernica je na Log. 0. Ak MASTER uvoľní SCL , musí monitorovať (počúvať) a môže taktovať Log. 1 až vtedy, keď všetci uvoľnia linku.

– **arbitráž:** Rieši kolízie na vodiči SDA. MASTER musí „počúvať“ či to, čo na linku nastavil, aj prečíta. Ak MASTER prečíta, iný stav ako nastavil, musí uvoľniť linku (prejsť do stavu SLAVE – čo ak je adresovaný ako SLAVE zariadenie?). Je zrejmé, že tento stav nastane, ak jeden MASTER vysiela log. 1 a druhý log. 0. „zvíťazí“ ten, ktorý vysiela na SDA log. 0.

TWI – ATmega48: registre

Bit Rate Generator Unit

This unit controls the period of SCL when operating in a Master mode. The SCL period is controlled by settings in the TWI Bit Rate Register (TWBR) and the Prescaler bits in the TWI Status Register (TWSR). Slave operation does not depend on Bit Rate or Prescaler settings, but the CPU clock frequency in the Slave must be at least 16 times higher than the SCL frequency. Note that slaves may prolong the SCL low period, thereby reducing the average TWI bus clock period. The SCL frequency is generated according to the following equation:

$$\text{SCL frequency} = \frac{\text{CPU Clock frequency}}{16 + 2(\text{TWBR}) \cdot (\mathit{PrescalerValue})}$$

- TWBR = Value of the TWI Bit Rate Register.
- *PrescalerValue* = Value of the prescaler.

Note: Pull-up resistor values should be selected according to the SCL frequency and the capacitive bus line load.

TWBR – TWI Bit Rate Register

Bit	7	6	5	4	3	2	1	0	
(0xB8)	TWBR7	TWBR6	TWBR5	TWBR4	TWBR3	TWBR2	TWBR1	TWBR0	TWBR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 7...0 – TWI Bit Rate Register**

TWBR selects the division factor for the bit rate generator. The bit rate generator is a frequency divider which generates the SCL clock frequency in the Master modes.

TWI – ATmega48: registre

TWCR – TWI Control Register

0 | 1

Bit	7	6	5	4	3	2	1	0	
(0xBC)	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE	TWCR
Read/Write	R/W	R/W	R/W	R/W	R	R/W	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The TWCR is used to control the operation of the TWI. It is used to enable the TWI, to initiate a Master access by applying a START condition to the bus, to generate a Receiver acknowledge, to generate a stop condition, and to control halting of the bus while the data to be written to the bus are written to the TWDR. It also indicates a write collision if data is attempted written to TWDR while the register is inaccessible.

TWINT – príznak prerušenia.

TWEA – riadi ACK bit.

TWSTA – „nastavenie“ Start bitu.

TWSTO – „nastavenie“ stoP bitu.

TWCC – príznak kolízneho zápisu do TWDR registra, ak je TWINT = Log. 0.

TWEN – „Zapnutie “ I2C (TWI). Riadenie pinov SCL a SDA preberá I2C.

–

TWIE – lokálne povolenie prerušenia (nezabudni na GI).

TWI – ATmega48: registre

TWSR – TWI Status Register

Bit	7	6	5	4	3	2	1	0
(0xB9)	TWS7	TWS6	TWS5	TWS4	TWS3	–	TWPS1	TWPS0
Read/Write	R	R	R	R	R	R	R/W	R/W
Initial Value	1	1	1	1	1	0	0	0

(TWSR and 0xF8)

- **Bits 7:3 – TWS: TWI Status**

These 5 bits reflect the status of the TWI logic and the 2-wire Serial Bus. The different status codes are described later in this section. Note that the value read from TWSR contains both the 5-bit status value and the 2-bit prescaler value. The application designer should mask the prescaler bits to zero when checking the Status bits. This makes status checking independent of prescaler setting. This approach is used in this datasheet, unless otherwise noted.

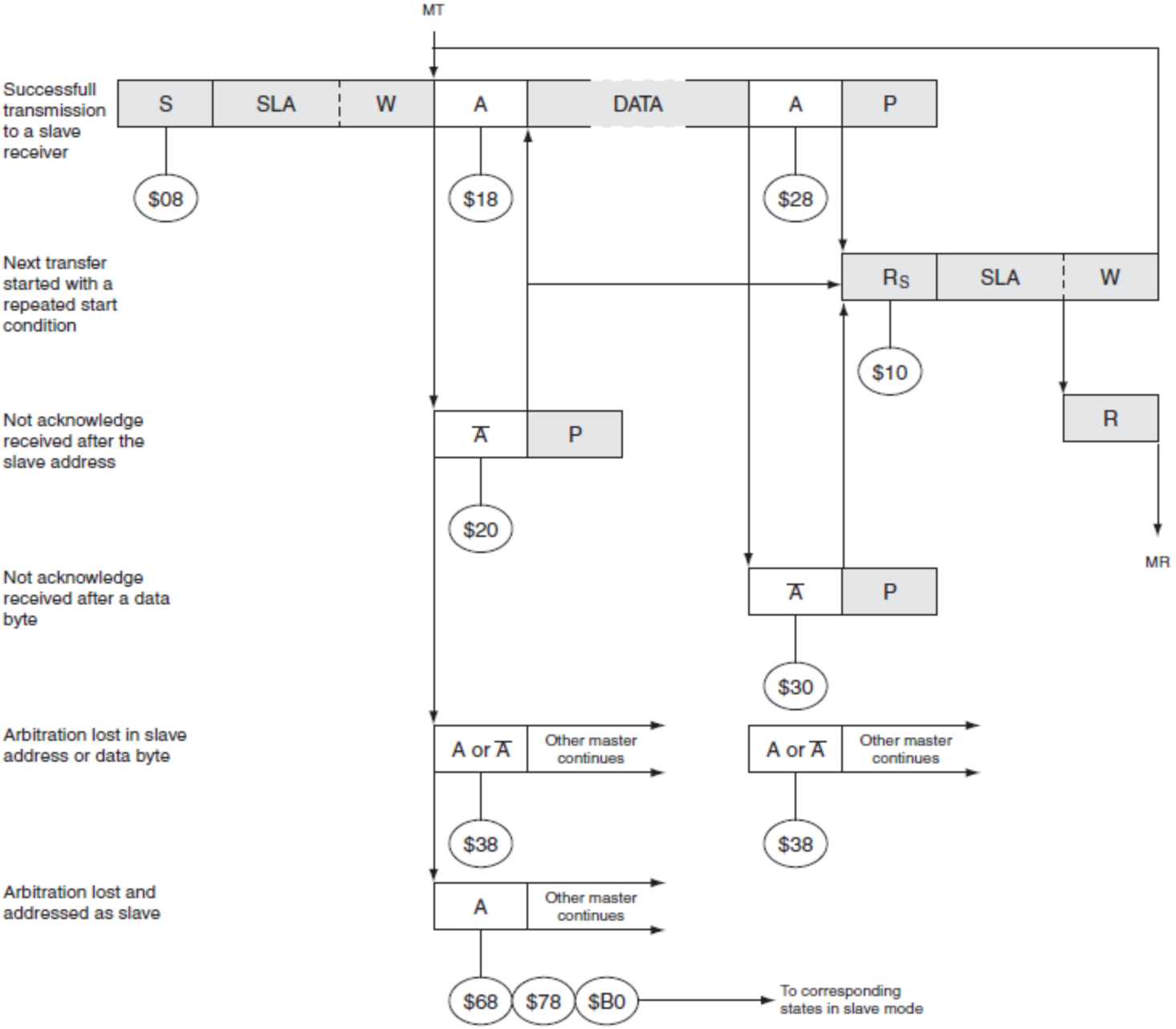
- **Bits 1:0 – TWPS: TWI Prescaler Bits**

These bits can be read and written, and control the bit rate prescaler.

Table 21-7. TWI Bit Rate Prescaler

TWPS1	TWPS0	Prescaler Value
0	0	1
0	1	4
1	0	16
1	1	64

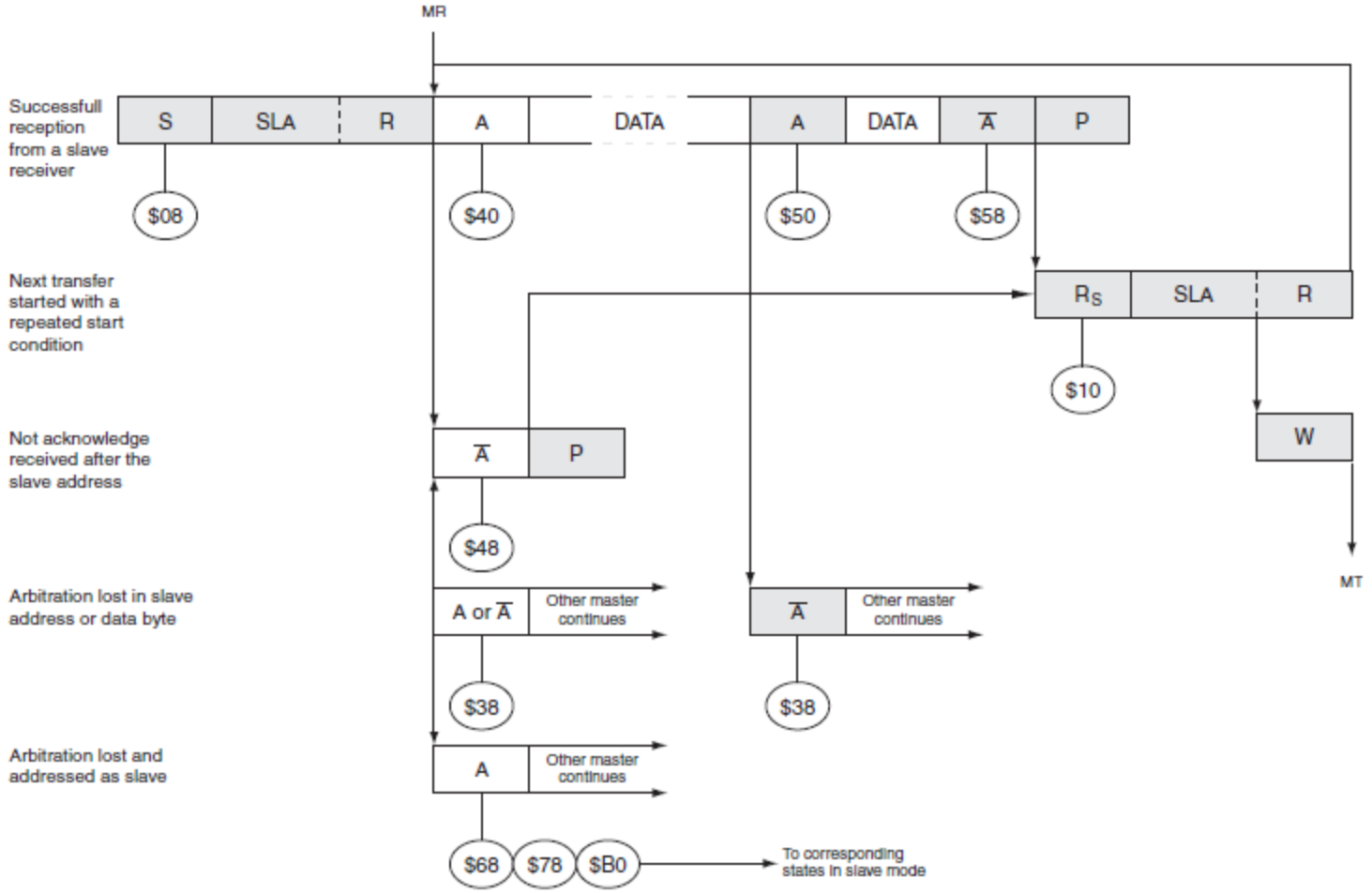
Formats and States in the Master Transmitter Mode



Status codes for Master Transmitter Mode

Status Code (TWSR) Prescaler Bits are 0	Status of the 2-wire Serial Bus and 2-wire Serial Interface Hardware	Application Software Response					Next Action Taken by TWI Hardware
		To/from TWDR	To TWCR				
			STA	STO	TWINT	TWEA	
0x08	A START condition has been transmitted	Load SLA+W	0	0	1	X	SLA+W will be transmitted; ACK or NOT ACK will be received
0x10	A repeated START condition has been transmitted	Load SLA+W or	0	0	1	X	SLA+W will be transmitted; ACK or NOT ACK will be received
		Load SLA+R	0	0	1	X	SLA+R will be transmitted; Logic will switch to Master Receiver mode
0x18	SLA+W has been transmitted; ACK has been received	Load data byte or	0	0	1	X	Data byte will be transmitted and ACK or NOT ACK will be received
		No TWDR action or	1	0	1	X	Repeated START will be transmitted
		No TWDR action or	0	1	1	X	STOP condition will be transmitted and TWSTO Flag will be reset
		No TWDR action	1	1	1	X	STOP condition followed by a START condition will be transmitted and TWSTO Flag will be reset
0x20	SLA+W has been transmitted; NOT ACK has been received	Load data byte or	0	0	1	X	Data byte will be transmitted and ACK or NOT ACK will be received
		No TWDR action or	1	0	1	X	Repeated START will be transmitted
		No TWDR action or	0	1	1	X	STOP condition will be transmitted and TWSTO Flag will be reset
		No TWDR action	1	1	1	X	STOP condition followed by a START condition will be transmitted and TWSTO Flag will be reset
0x28	Data byte has been transmitted; ACK has been received	Load data byte or	0	0	1	X	Data byte will be transmitted and ACK or NOT ACK will be received
		No TWDR action or	1	0	1	X	Repeated START will be transmitted
		No TWDR action or	0	1	1	X	STOP condition will be transmitted and TWSTO Flag will be reset
		No TWDR action	1	1	1	X	STOP condition followed by a START condition will be transmitted and TWSTO Flag will be reset
0x30	Data byte has been transmitted; NOT ACK has been received	Load data byte or	0	0	1	X	Data byte will be transmitted and ACK or NOT ACK will be received
		No TWDR action or	1	0	1	X	Repeated START will be transmitted
		No TWDR action or	0	1	1	X	STOP condition will be transmitted and TWSTO Flag will be reset
		No TWDR action	1	1	1	X	STOP condition followed by a START condition will be transmitted and TWSTO Flag will be reset
0x38	Arbitration lost in SLA+W or data bytes	No TWDR action or	0	0	1	X	2-wire Serial Bus will be released and not addressed Slave mode entered
		No TWDR action	1	0	1	X	A START condition will be transmitted when the bus becomes free

Formats and States in the Master Receiver Mode



Status codes for Master Receiver Mode

Status Code (TWSR) Prescaler Bits are 0	Status of the 2-wire Serial Bus and 2-wire Serial Interface Hardware	Application Software Response					Next Action Taken by TWI Hardware
		To/from TWDR	To TWCR				
			STA	STO	TWINT	TWEA	
0x08	A START condition has been transmitted	Load SLA+R	0	0	1	X	SLA+R will be transmitted ACK or NOT ACK will be received
0x10	A repeated START condition has been transmitted	Load SLA+R or	0	0	1	X	SLA+R will be transmitted ACK or NOT ACK will be received
		Load SLA+W	0	0	1	X	SLA+W will be transmitted Logic will switch to Master Transmitter mode
0x38	Arbitration lost in SLA+R or NOT ACK bit	No TWDR action or	0	0	1	X	2-wire Serial Bus will be released and not addressed Slave mode will be entered
		No TWDR action	1	0	1	X	A START condition will be transmitted when the bus becomes free
0x40	SLA+R has been transmitted; ACK has been received	No TWDR action or	0	0	1	0	Data byte will be received and NOT ACK will be returned
		No TWDR action	0	0	1	1	Data byte will be received and ACK will be returned
0x48	SLA+R has been transmitted; NOT ACK has been received	No TWDR action or	1	0	1	X	Repeated START will be transmitted
		No TWDR action or	0	1	1	X	STOP condition will be transmitted and TWSTO Flag will be reset
		No TWDR action	1	1	1	X	STOP condition followed by a START condition will be transmitted and TWSTO Flag will be reset
0x50	Data byte has been received; ACK has been returned	Read data byte or	0	0	1	0	Data byte will be received and NOT ACK will be returned
		Read data byte	0	0	1	1	Data byte will be received and ACK will be returned
0x58	Data byte has been received; NOT ACK has been returned	Read data byte or	1	0	1	X	Repeated START will be transmitted
		Read data byte or	0	1	1	X	STOP condition will be transmitted and TWSTO Flag will be reset
		Read data byte	1	1	1	X	STOP condition followed by a START condition will be transmitted and TWSTO Flag will be reset

TWI – ATmega48: registre

TWDR – TWI Data Register

Bit	7	6	5	4	3	2	1	0	
(0xBB)	TWD7	TWD6	TWD5	TWD4	TWD3	TWD2	TWD1	TWD0	TWDR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	1	1	1	1	1	1	1	1	

In Transmit mode, TWDR contains the next byte to be transmitted. In Receive mode, the TWDR contains the last byte received. It is writable while the TWI is not in the process of shifting a byte. This occurs when the TWI Interrupt Flag (TWINT) is set by hardware. Note that the Data Register cannot be initialized by the user before the first interrupt occurs. The data in TWDR remains stable as long as TWINT is set. While data is shifted out, data on the bus is simultaneously shifted in. TWDR always contains the last byte present on the bus, except after a wake up from a sleep mode by the TWI interrupt. In this case, the contents of TWDR is undefined. In the case of a lost bus arbitration, no data is lost in the transition from Master to Slave. Handling of the ACK bit is controlled automatically by the TWI logic, the CPU cannot access the ACK bit directly.

- **Bits 7:0 – TWD: TWI Data Register**

These eight bits constitute the next data byte to be transmitted, or the latest data byte received on the 2-wire Serial Bus.

TWI – ATmega48: registre

TWAR – TWI (Slave) Address Register

Bit	7	6	5	4	3	2	1	0	
(0xBA)	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	TWAR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	1	1	1	1	1	1	1	0	

The TWAR should be loaded with the 7-bit Slave address (in the seven most significant bits of TWAR) to which the TWI will respond when programmed as a Slave Transmitter or Receiver, and not needed in the Master modes. In multi master systems, TWAR must be set in masters which can be addressed as Slaves by other Masters.

The LSB of TWAR is used to enable recognition of the general call address (0x00). There is an associated address comparator that looks for the slave address (or general call address if enabled) in the received serial address. If a match is found, an interrupt request is generated.

- **Bits 7:1 – TWA: TWI (Slave) Address Register**
- **Bit 0 – TWGCE: TWI General Call Recognition Enable Bit**

If set, this bit enables the recognition of a General Call given over the 2-wire Serial Bus.

TWAMR – TWI (Slave) Address Mask Register

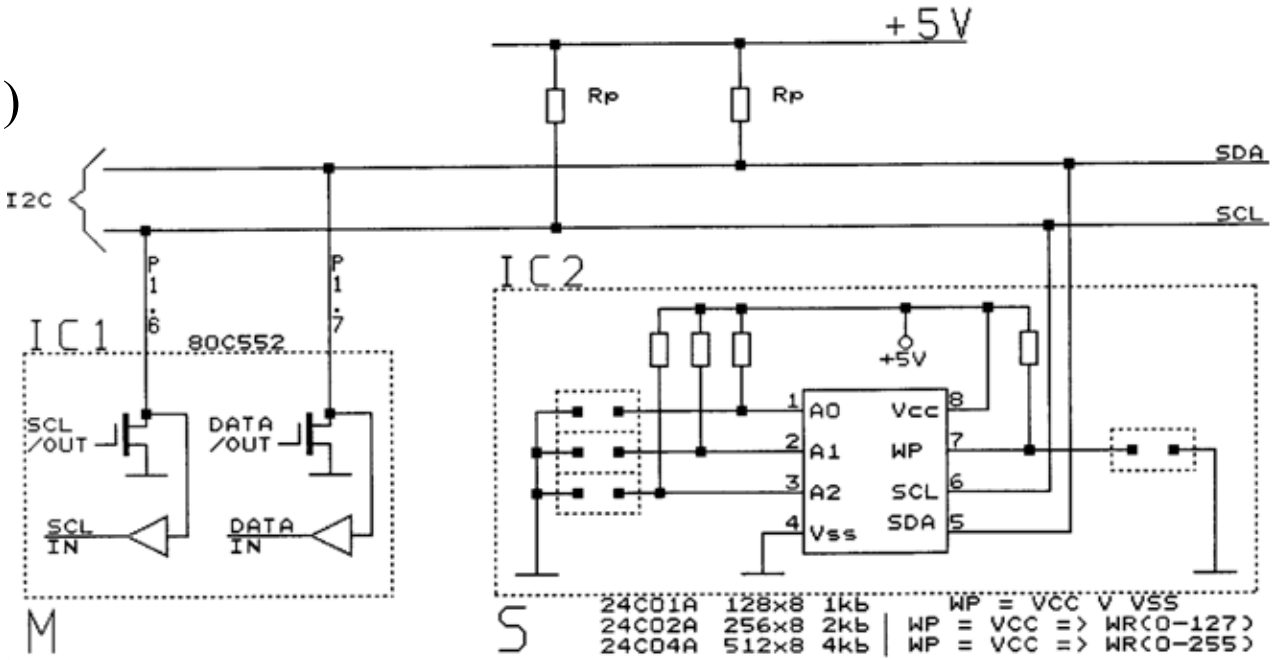
Bit	7	6	5	4	3	2	1	0	
(0xBD)	TWAM[6:0]							–	TWAMR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	
Initial Value	0	0	0	0	0	0	0	0	

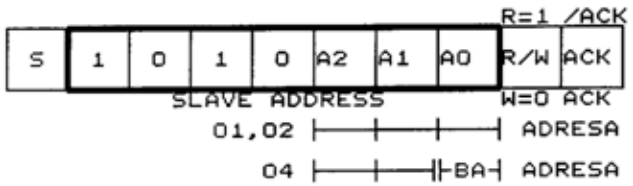
- **Bits 7:1 – TWAM: TWI Address Mask**

The TWAMR can be loaded with a 7-bit Salve Address mask. Each of the bits in TWAMR can mask (disable) the corresponding address bits in the TWI Address Register (TWAR). If the mask bit is set to one then the address match logic ignores the compare between the incoming address bit and the corresponding bit in TWAR. Figure 21-22 shown the address match logic in detail.

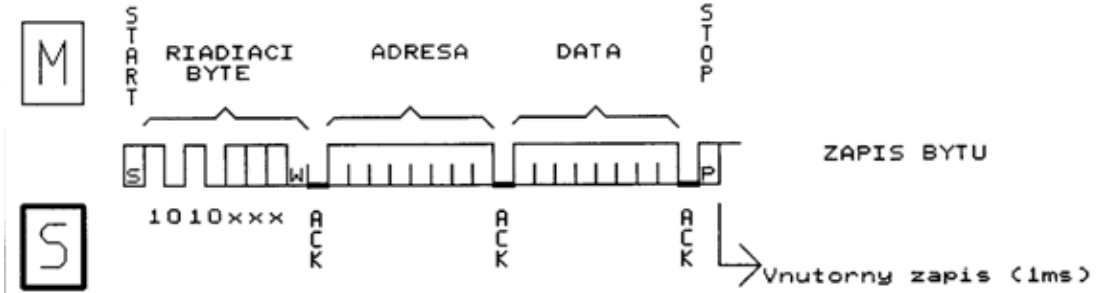
I2C – pripojenie EEPROM

Piny:
1,2,3:Adresa IC (max 8)
4: V_{SS}
5: SDA
6:SCL
7:WP = log. 1
8: V_{CC}

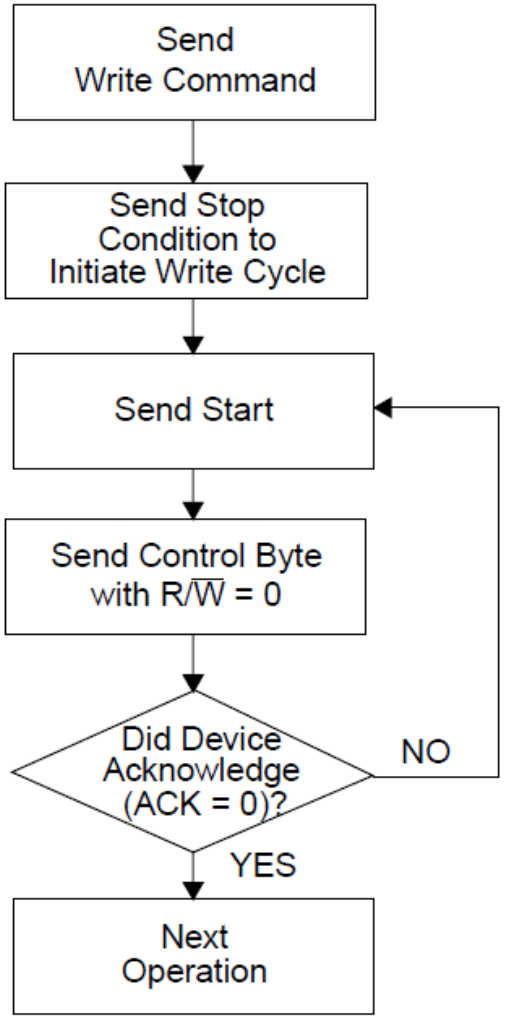




EEPROM majú vnútorný AC, ktorý sa automaticky inkrementuje



“ACKNOWLEDGE POLLING”



I2C – pripojenie EEPROM