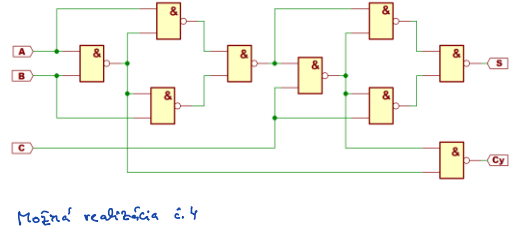
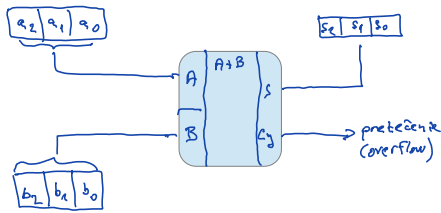


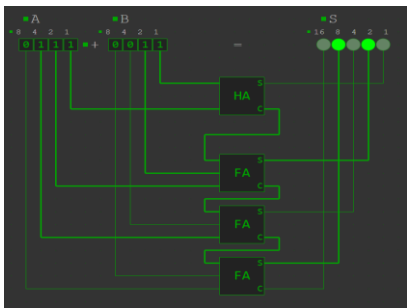
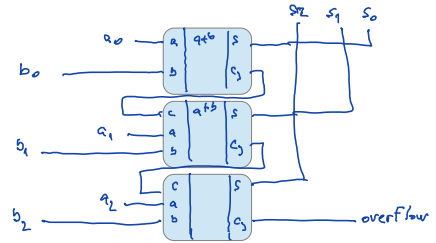
Úplná sčítačka - realizácia len z NAND



3-bitová sčítačka



3-bitová sčítačka



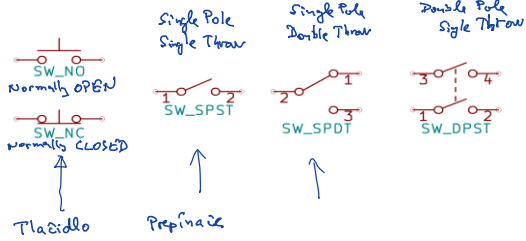
<https://simulator.io/board/VuE4wWhzhF/4>

Spínač

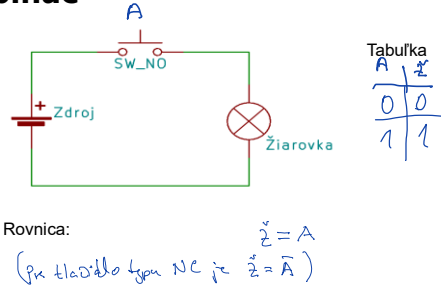


Source: Wikipedia

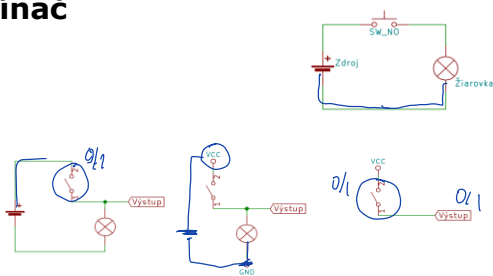
Spínač



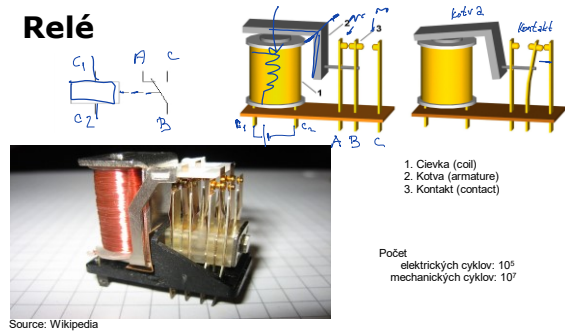
Spínač



Spínač



Relé



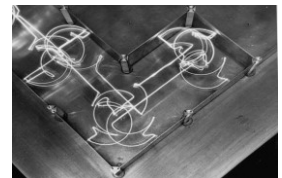
Claude Elwood Shannon

* 30. apríla 1916, Michigan
† 24. február 2001, Massachusetts
– profesor na MIT
Kybernetika, Teória informácie, Entropia
Symbolická analýza zmeny a spínacie obvody
Bell Labs Inc. - relová logika



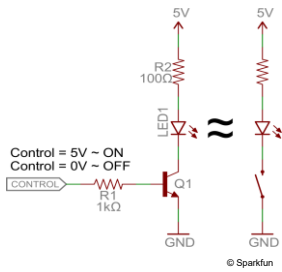
Source: Wikipedia, <http://cyberneticzoo.com>

Theseus: Maze-Solving Mouse (1952)



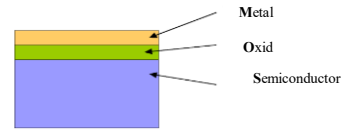
Source: <http://cyberneticzoo.com>

Tranzistor



Tranzistor unipolárny

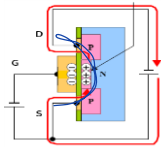
Súčasnne počítače využívajú unipolárne tranzistory
FET – Field Effect Transistor



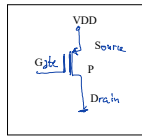
Metal Oxid Semiconductor (MOS)

PMOS (MOS tranzistor s kanálom P)

- historicky najstaršia technológia:
- nevýhody: nízka rýchlosť a zlá zlučiteľnosť s TTL obvodymi

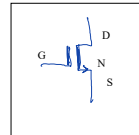


Náhrada: NMOS (MOS tranzistor s kanálom N).

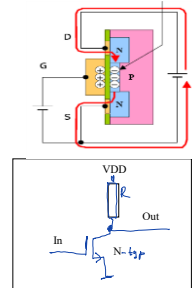


Technológia NMOS

Výhody: rýchlejšie, zlučiteľné s TTL
Nevýhody: „straty“

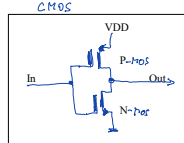


Náhrada: CMOS



Technológia CMOS (Complementary MOS)

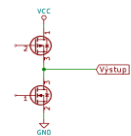
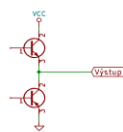
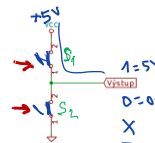
Výhody:
minimalizované straty
zlučiteľné s TTL



Logické úrovne:

- log. 0 = 0,0 až $0,3 \times V_{DD}$ Ak $V_{DD} = 5,0V$ je to 0 až 1,5 V
- log. 1 = $0,7 \times V_{DD}$ až V_{DD} Ak $V_{DD} = 5,0V$ je to 3,5 až 5,0 V
- Okrem $V_{DD} = 5,0V$ sa používa aj $V_{DD} = 3,3V$ a $V_{DD} = 2,9V$ a iné.

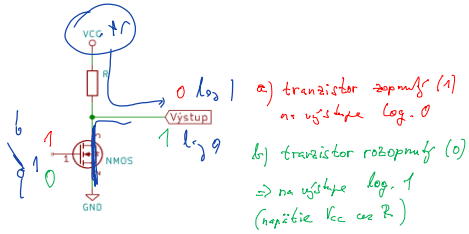
Totem pole



1. $S_1 = 0 \Rightarrow R_{eq} \uparrow$
 2. $S_2 = 0 \Rightarrow R_{eq} = 0$
 3. $S_1 = S_2 = 0 \Rightarrow$ Trieb. stav
 $R_{eq} \uparrow$ a vysoká impedancia
 4. $S_1 = S_2 = 0 \Rightarrow$ s KRAAT! (nechame!)

S CMOS tranzistormi

Integrovaný obvod



12. 9. 1958
 Americký fyzik Jack Kilby
 vytvoril prvý integrovaný
 obvod na jednom čípe
 2000 - Nobel Prize in
 physics

Integrovaný obvod



Name	Signification	Year	Transistors number ⁽¹⁾	Logic gates number ⁽¹⁾
SSI	small-scale integration	1964	1 to 10	1 to 12
MSI	medium-scale integration	1968	10 to 500	13 to 99
LSI	large-scale integration	1971	500 to 20,000	100 to 9,999
VLSI	very large-scale integration	1980	20,000 to 1,000,000	10,000 to 99,999
ULSI	ultra-large-scale integration	1984	1,000,000 and more	100,000 and more

Moorov zákon

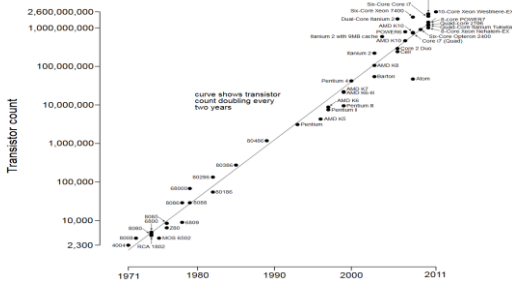
Gordon Moore
 spoluzakladateľ firiem Intel
 a Fairchild Semiconductor



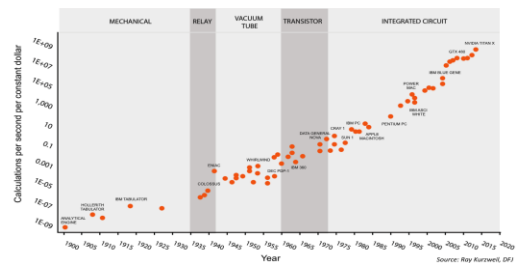
Moore's law is the observation:

*The number of transistors in a dense integrated circuit **doubles** approximately every **two years** (1965)*

Moorov zákon



120 Years of Moore's Law



Moorov zákon

Ak by sa rovnako rozvíjal automobilový priemysel:

300 000 km/h

850 000 km / liter

0,04 \$ / ks



7400

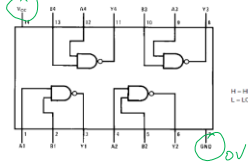
TTL (Transistor-Transistor-Logic)
 Integrovaný obvod 4x 2-vst. NAND
 Technológia SSI – obsahuje cca 16 tranzistorov a ďalšie súčiastky
 Cena cca 0,30 \$ ale bola aj 22\$ r. 1965

Nie Intel Core i5-7400 Quad-Core, 3,0 GHz (65 W), TurboBoost 3,5 GHz, Intel HD Graphics 630 (1000 MHz), 6 MB L3 cache, socket 1151, Kaby lake 14 nm
 192 USD Transistorov: 750 000 000



SN7400

Connection Diagram



High = log. 1
 Low = log. 0

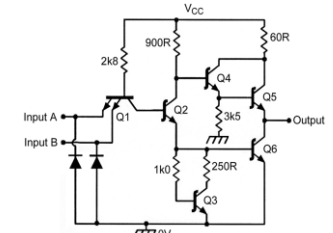
Function Table

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

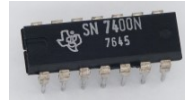
H = HIGH Logic Level = 1
 L = LOW Logic Level = 0



SN7400



Vnitrová zapojenie jedného NAND stena



Katalógový list
 = datasheet

DM74LS00

Absolute Maximum Ratings (Note 1)

Supply Voltage: 0V to +5.5V
 Operating Free Air Temperature Range: 0°C to +70°C
 Storage Temperature Range: -65°C to +150°C

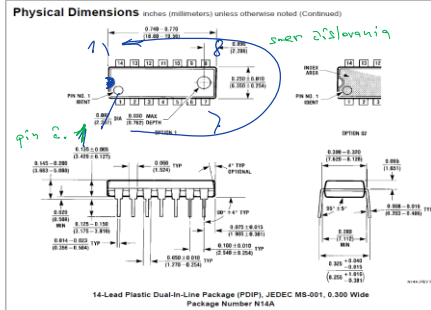
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V _{CC}	Supply Voltage	0	5	5.5	V
V _{OL}	LOW Level Input Voltage	0	0.8	1	V
V _{OH}	HIGH Level Output Voltage	2.7	3.4	5	V
I _{OL}	LOW Level Output Current	0	0.5	20	mA
I _{OH}	HIGH Level Output Current	0	0.5	20	mA
T _A	Free Air Operating Temperature	0	70	70	°C

Electrical Characteristics
 over recommended operating free air temperature range (unless otherwise noted)

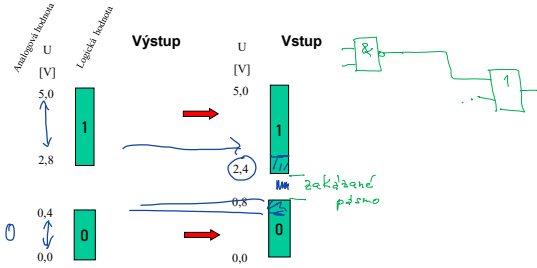
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -10 mA			-1.5	V
V _{OL}	HIGH Level Input Voltage	V _{CC} = Min, I _{OL} = Max, V _I = Max			1	V
V _{OL}	LOW Level Output Voltage	V _{CC} = Min, I _{OL} = Max, V _I = Min	0.35	0.5	0.5	V
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = V _I	0.25	0.4	0.1	mA
I _{OL}	LOW Level Input Current	V _{CC} = Max, V _I = 0 V			-30	mA
I _{OH}	HIGH Level Input Current	V _{CC} = Max, V _I = 5 V			-30	mA
I _{OL}	LOW Level Output Current	V _{CC} = Max, V _O = 0.4 V			-30	mA
I _{OH}	HIGH Level Output Current	V _{CC} = Max, V _O = 5 V			-30	mA
I _{OL}	Input Current with Outputs HIGH	V _{CC} = Max	0.8	1.5	0.8	mA

interný zapojenie obvodu!

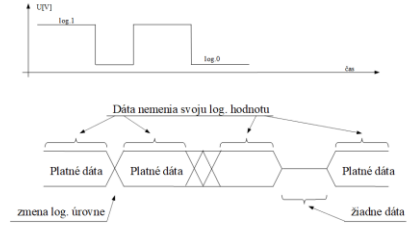


DM74LS00 Quad 2-Input NAND Gate

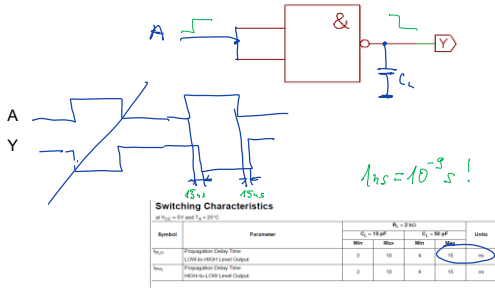
TTL obvody: logické úrovne



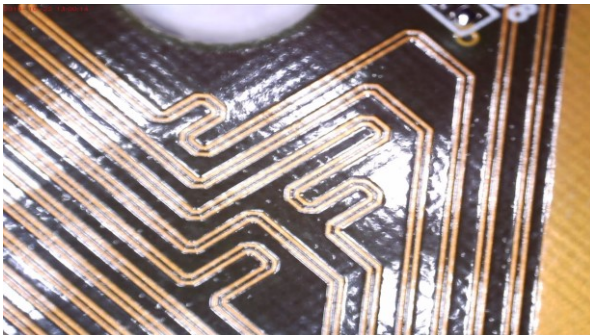
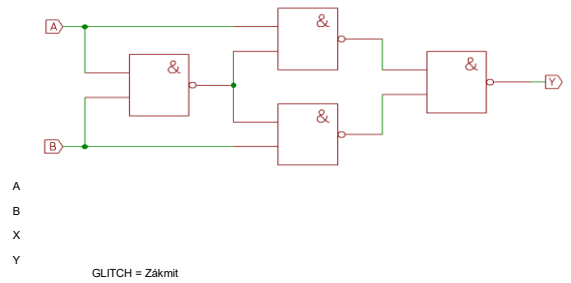
Časové diagramy



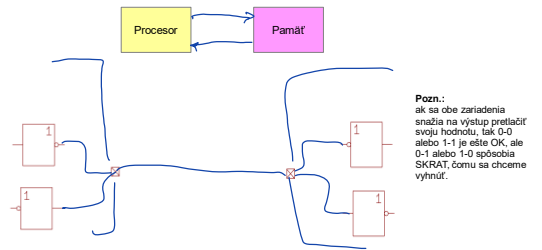
Oneskorenie



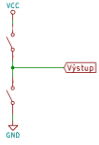
Oneskorenie



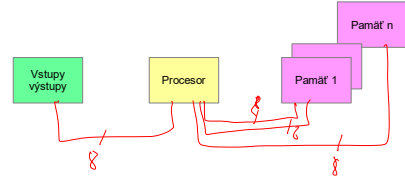
Zbernice – obojsmerný V/V



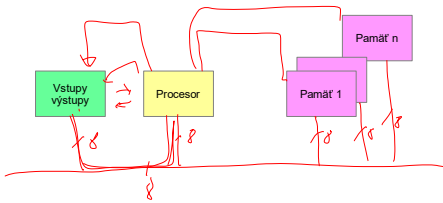
Zbernice – obojsmerný V/V



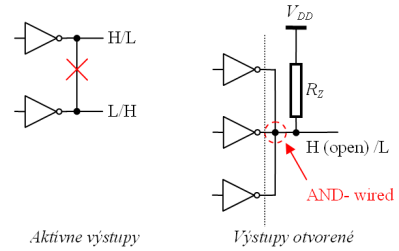
Zbernica – trojstavový výstup



Zbernica – trojstavový výstup



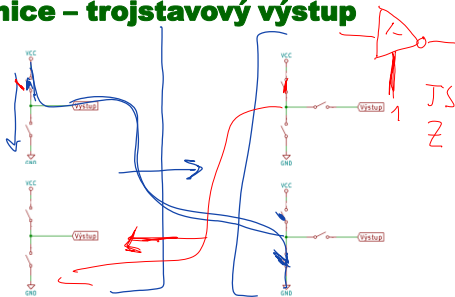
Spájanie vstupov a výstupov



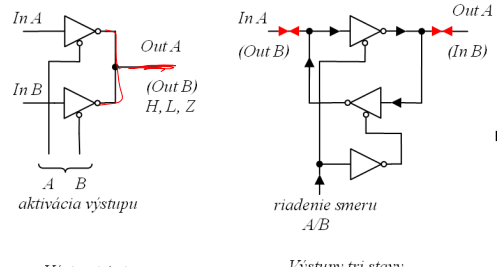
Aktívne výstupy

Výstupy otvorené

Zbernica – trojstavový výstup



Zbernica



aktivácia výstupu

riadenie smeru A/B

Chcem vedieť viac...

John F. WAKERLY:
Digital design.
Stanford University : Prentice Hall, 2006.



Jean-Michel BERNARD, Jean HUGON
a Robert Le Corvec:
Od logických obvodů k mikroprocesorům.
SNTL : Praha, 1982

